Final Project Report

on

DESIGN, DEVELOPMENT, AND DELIVERY OF 75-VA INTEGRATED STATIC INVERTER

For Period

April 1965 through April 1967

Contract No. NAS8-11925

Control No. DCN 1-5-40-56195 (1F) & S1 (1F)

Prepared by

TEXAS INSTRUMENTS INCORPORATED
Semiconductor-Components Division
P. O. Box 5012
Dallas, Texas 75222

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
George C. Marshall Space Flight Center
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ABSTRACT

The 75-VA static inverter is a 28-V dc to 3ϕ sine-wave 400-Hz inverter designed for use as a gyro platform power supply. The basic circuit approach, which uses the technique of synthesizing a sine wave from a step-approximated waveshape, was developed by NASA Huntsville.

It has excellent performance characteristics such as high efficiency (67 percent), good voltage regulation, and frequency stability; protection against damage by short circuits and overloads, and capability of operation over a wide ambient temperature range.

The contract was awarded to TI for the design, development, and fabrication of one breadboard and three production-model 75-VA static inverters. Emphasis was to be placed on the use of integrated circuit arrays and integrated or multiple-chip power transistor packages wherever possible, to increase reliability and reduce weight and volume.

The report describes the circuitry, fabrication details, and overall inverter performance characteristics. Also considerable attention is devoted to operational characteristics and fabrication details of the three integrated-circuit arrays and the two types of dual-chip power transistors which were fabricated for the inverter.

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

This report's Supplement, published simultaneously under separate cover, comprises four exhibits, as follows: A, Isolated Common Terminal (Assembly Drawing); B, Power Transistor Mechanical Drawings; C, Single Chip Johnson Counter Information; D, Potted Assembly and Inverter Package Information.

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

SECTION I

SYSTEM DESCRIPTION

The inverter discussed in this report is a 75-VA platform power supply using state-of-the-art integrated components. The inverter uses digital circuitry in developing the sine wave and for its regulation in order to achieve high efficiency.

The basic approach of utilizing digital techniques and unique transformer connections, as applied by NASA at Marshall Space Flight Center, was used successfully to develop several higher-power inverters. As platform power requirements were reduced because of advances in semiconductor technologies, MSFC realized that the next logical advance in an inverter would be large-scale integration. An RFQ released to industry provided broad guidelines for such an inverter with a 75-VA output capability Texas Instruments was selected to develop, fabricate, and deliver the three production models of this unit.

The inverter has the following capabilities and characteristics:

1) Input: 25 to 30 V dc.
2) Output: 3ϕ, 26 V ac with ±0.2 V regulation from no load to full load; also 4.8-kHz, 1.92-kHz, and 1.6-kHz, 50-percent-duty cycle-pulse trains (20 V amplitude and $Z_O = 400\ \Omega$).
3) Frequency tolerance: 400 Hz ± 0.0015-percent tolerance for 3ϕ outputs. Same tolerance also on three pulse-train outputs.
4) Load recovery time: No load to full load in 10 ms.
5) Overload: Capable of supplying 150 percent of rated load continuously; 3ϕ outputs are current limited.
6) Short circuit: Current limiting provides protection against single ϕ and 3ϕ short circuits.

7) Power factor: Inverter is capable of handling a 50-percent lagging power factor load.

8) Ambient temperature: Inverter is capable of operating from -25°C to +125°C.

9) Waveform distortion: Less than 5 percent THD.

10) Efficiency: 66 percent.

11) Case and packaging description: The external case, 10 inches long by 8-1/2 wide by 4-5/8 deep, consists of a one-piece housing and separate cover machined from 6061-T6 sheet aluminum. The case has a hard, black anodized finish. The cover, attached to the top side of the case, is pressure sealed by a silicon O-ring gasket. Two valves, for purging and filling, are provided. Three external M-S connectors are mounted on the same face as the purge valves.

The unit contains nine hard, black anodized-aluminum transformer and capacitor assemblies, two etched-circuit assemblies, an isolated common terminal, eight stud-mounted transistors, a stud-mounted diode, and a stainless-steel filter assembly. The entire unit weighs 18 pounds, 3-3/4 ounces.

(12) Case and packaging design goals:

a) Shock: 500 g, 1 ms (exception: TXCO, 100 g, 10 ms).

b) Vibration: 20 g, 100 to 2000 Hz.

c) Vacuum pressurization: The inverter case is capable of pressurization to 30 PSIG at sea level. However, the type of external M-S connectors used as recommended exhibits a rather large leak rate despite potting.

d) Radiation: Inverter to be operable within flight tolerance during and after exposure to 1×10^{11} NVT ($E \geq 5$ MEV) and 1×10^5 R. Maximum exposure rates to be 1×10^5 R/hr and 1×10^{11} neutron/cm^2/hr.

(13) Inverter reliability: The inverter was designed and built with the intent of achieving a reliability goal of 0.999 based on a 100-hour orbital mission.

SECTION II
CIRCUITRY

A. BASIC APPROACH

Function of the inverter is to convert unregulated dc voltage into regulated 3ϕ ac voltage. The simplified block diagram in Figure 1 shows the inverter divided into three main sections. The technique used for the basic-inverter section is one developed by NASA Huntsville. Briefly stated, the approach is to employ a digital technique to obtain a 3ϕ step-approximated sine-wave wave having low harmonic content (no harmonics below the 11th) and therefore easily filtered. Since the waveshapes

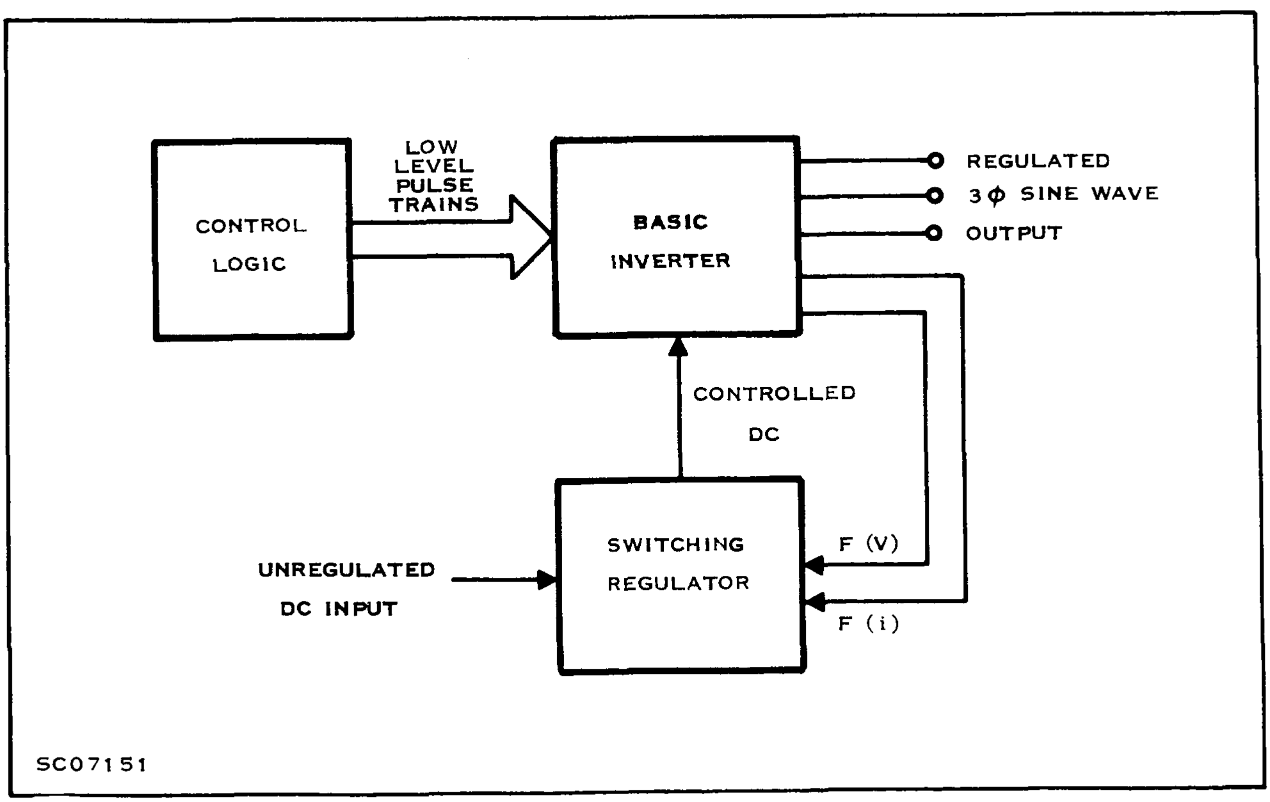


Figure 1. Simplified Block Diagram

are generated by transistors operating in a switching mode, circuit efficiency is much greater than could be obtained from an inverter technique which required the transistors to operate in a linear mode.

In Figure 2 the V_{AB} waveform represents the output waveform obtained from the basic inverter before filtering. (This is an easy-to-work-with approximation to the ideal step-approximated waveshape given in Appendix A.)

The waveshape in Figure 2 is obtained by summing the square waves shown in the same figure, i.e., V_{A1}, V_{B1}, V_{C1}, etc. Waveshapes for the other two phases (identical except for phase shift) can be obtained by adding a different combination of square waves as noted in Figures 3 and 4. The square waves are generated and summed as shown in Figure 5. The Johnson Counter is a six-flip-flop shift register in which each flip-flop has its output shifted 30° from the preceding output. Two outputs are taken from each flip-flop, each pair being connected to a push-pull pair of darlingtons. The power transistors and transformers amplify the Johnson Counter outputs and convert them to ac square waves.

Each transformer has three different secondaries, and consequently three different-magnitude square waves are generated. By correctly connecting the proper secondary windings from each transformer the desired phase voltage is obtained. Each of these three series windings is then connected to form a three-wire delta system; choice of delta was arbitrary. A wye connection could have been made, with the only difference being in the resulting magnitude of phase voltage and current.

A better understanding of the complete inverter is conveyed by the more detailed block diagram shown in Figure 6. A 2.4576-MHz temperature-compensated crystal oscillator (TXCO) is in effect the master "clock" for the whole inverter. All outputs from the inverter are derived by digital countdown techniques from the oscillator

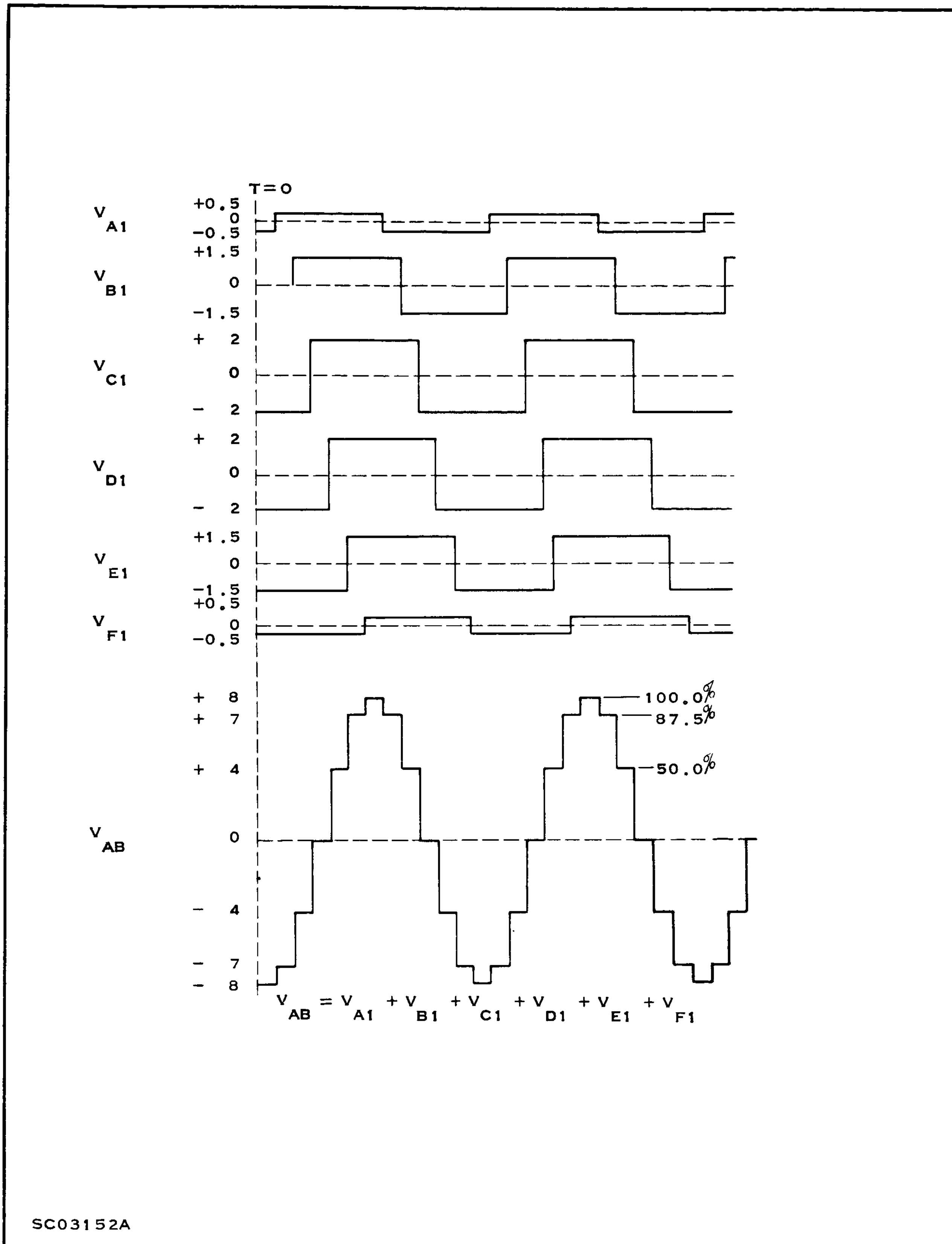
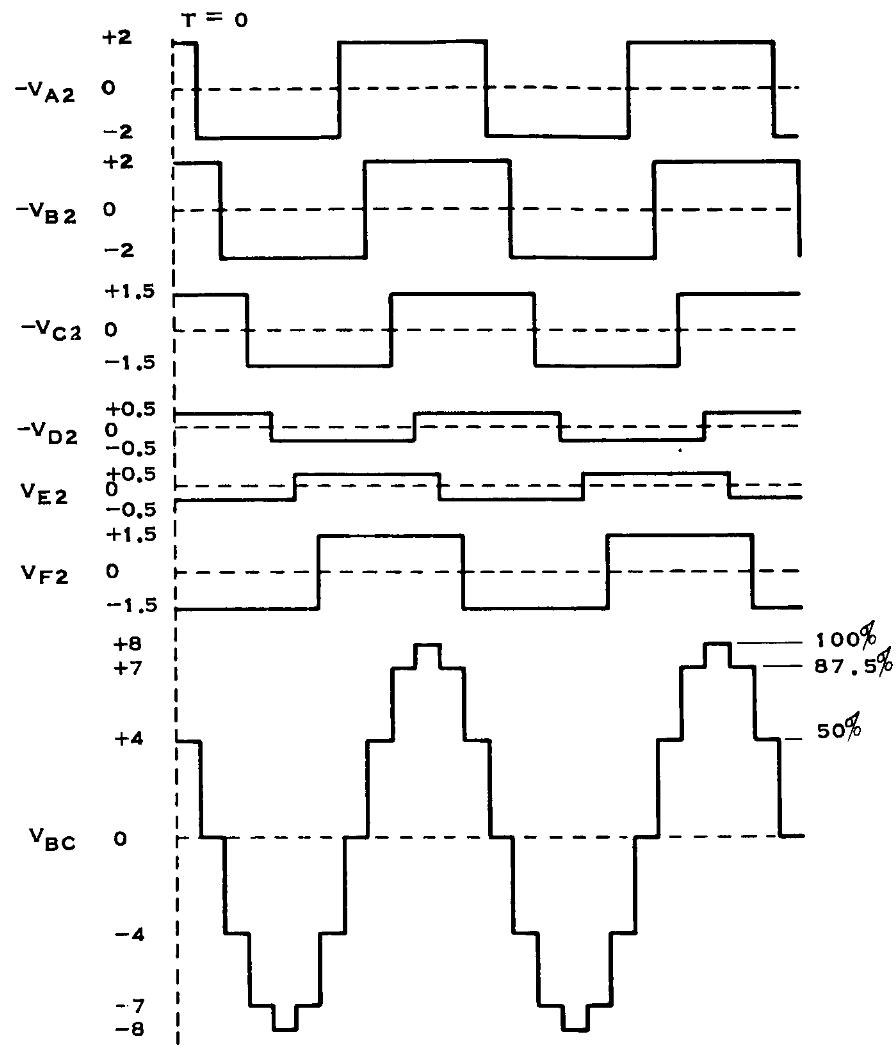


Figure 2. Waveforms — First Phase



$$V_{BC} = -V_{A2} - V_{B2} - V_{C2} - V_{D2} + V_{E2} + V_{F2}$$

Figure 3. Waveforms — Second Phase

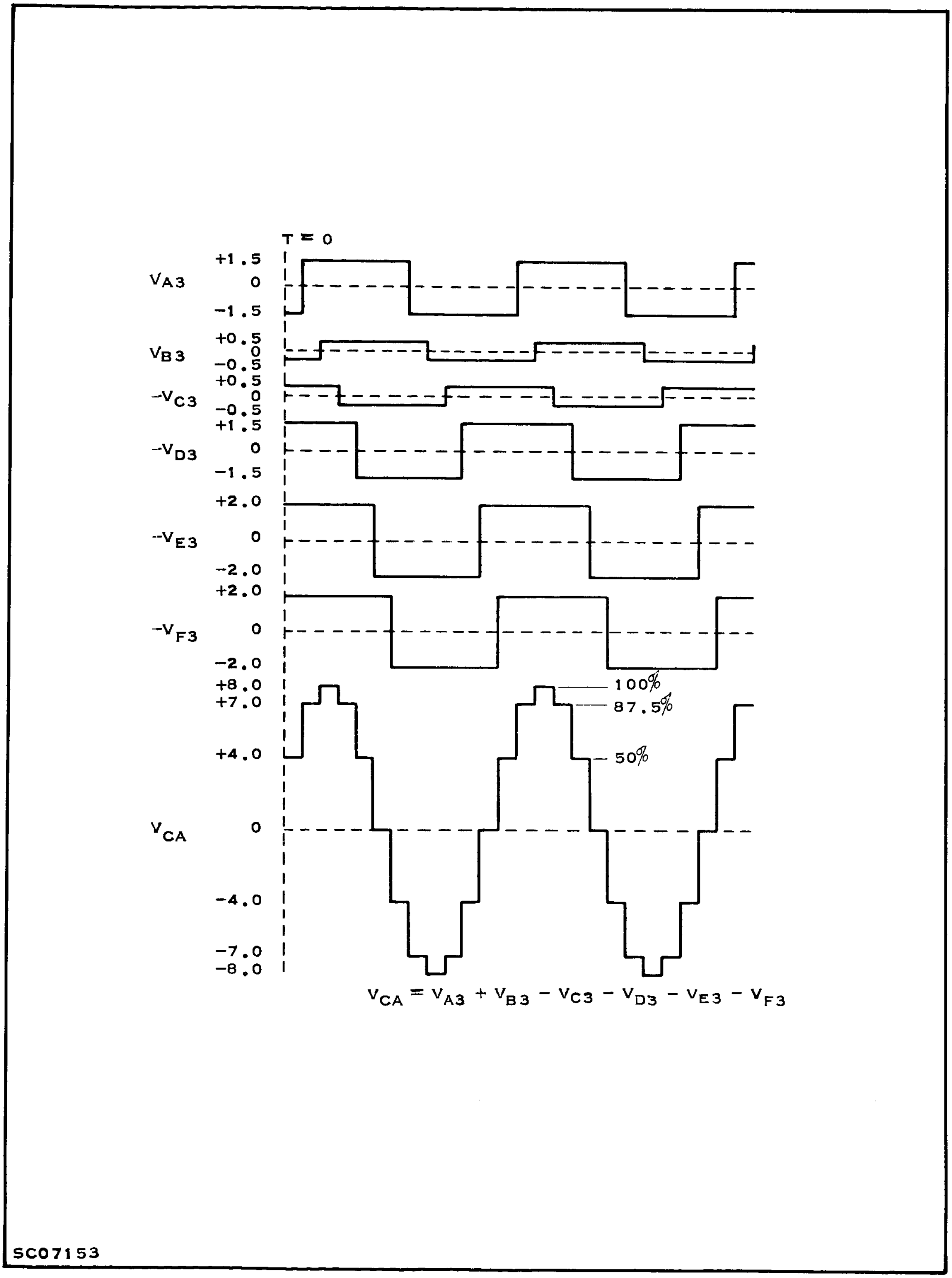


Figure 4. Waveforms — Third Phase

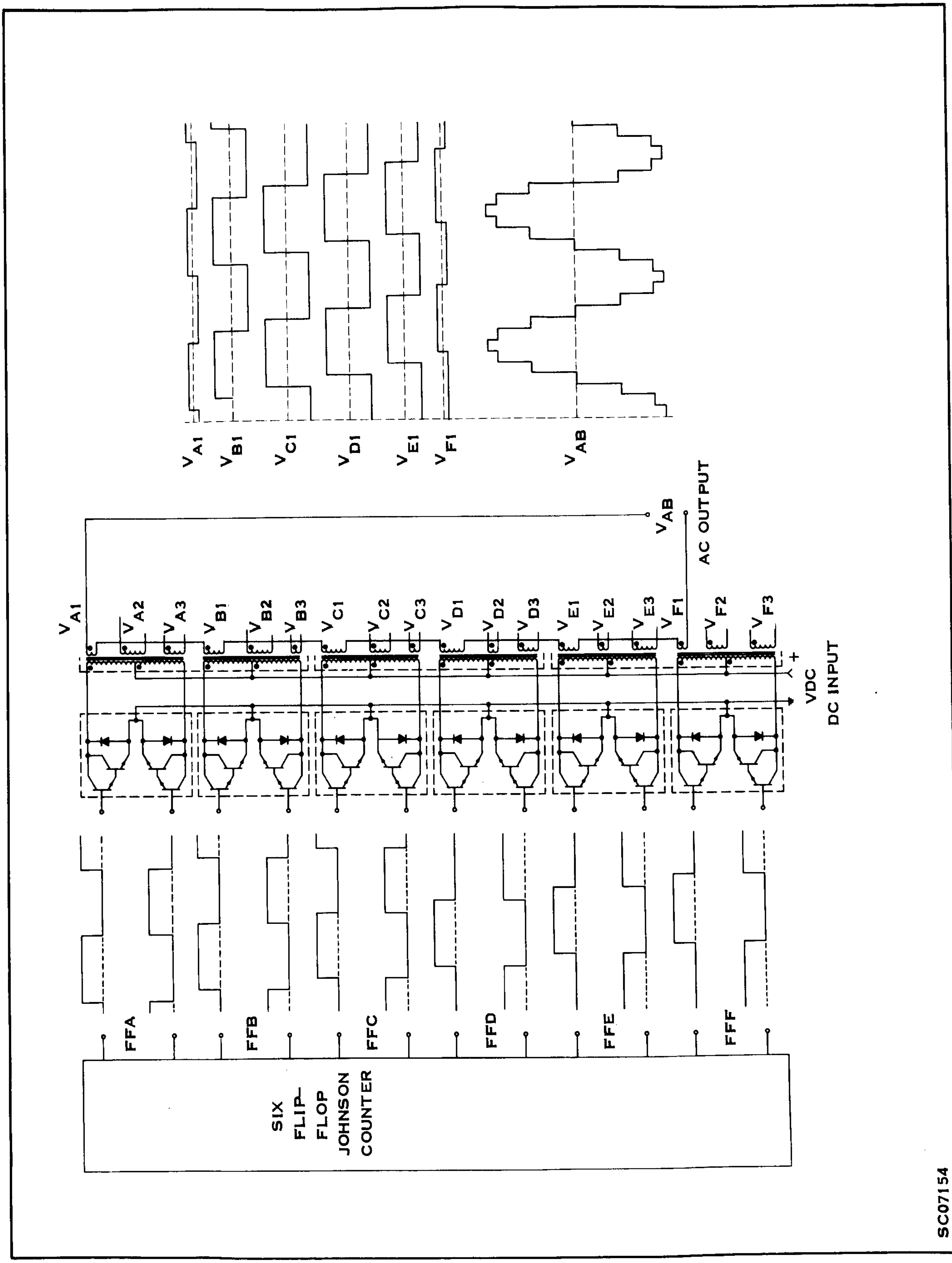


Figure 5. Basic Inverter

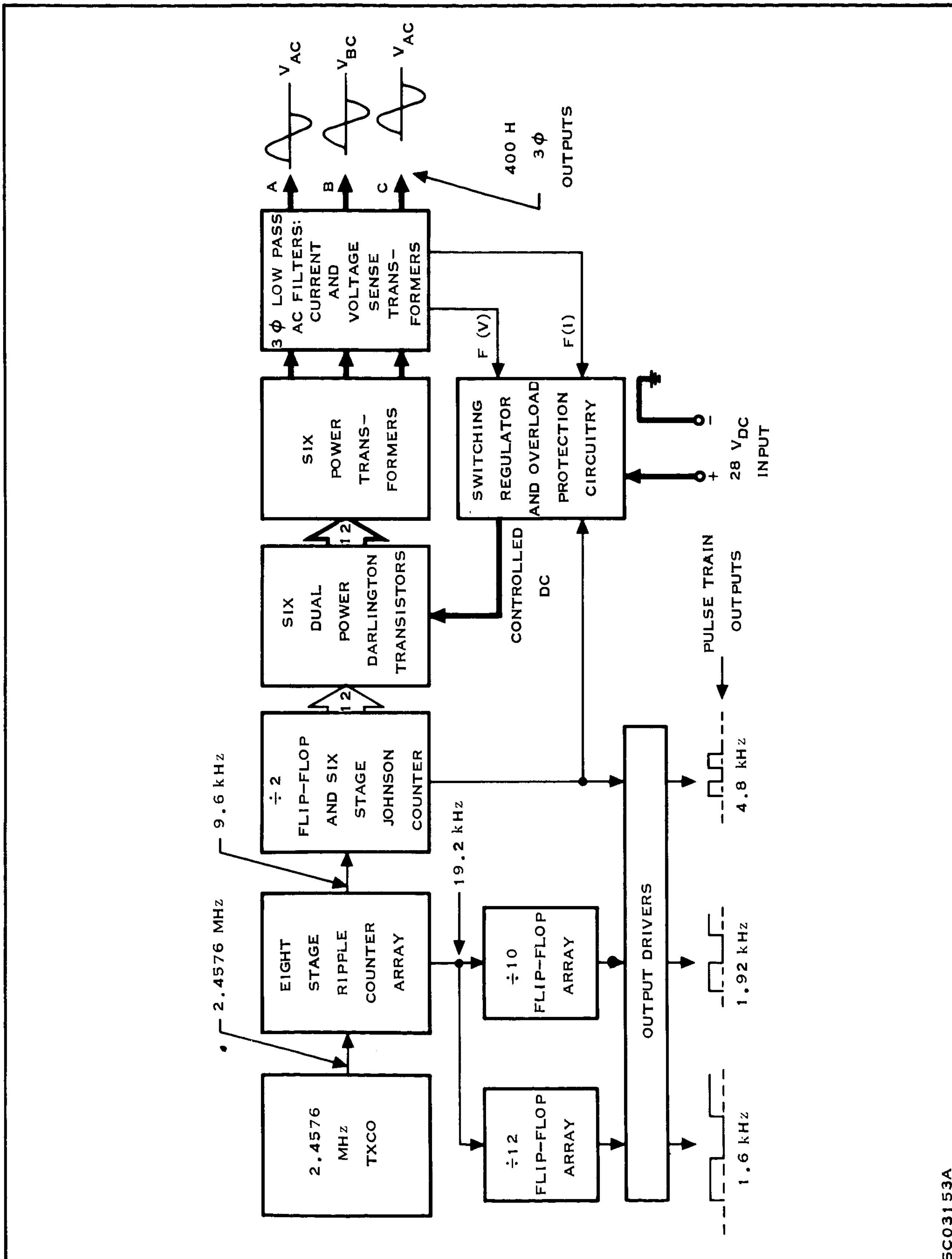


Figure 6. Block Diagram

output. The output is fed into an integrated-circuit ripple counter array (L-166) which has two outputs — one representing the input signal divided by 2^7 or 19.2 kHz, and the other the input signal divided by 2^8 or 9.6 kHz. Both are 50-percent duty-cycle pulse trains. The 19.2-kHz pulse train is then fed into both ÷10 and ÷12 integrated-circuit flip-flop arrays.

The 9.6-kHz pulse train is fed into an SN5300 integrated-circuit toggle flip-flop which performs a ÷2 function. The outputs of the ÷12, ÷10, and ÷2 circuits are 1.6 kHz, 1.92 kHz, and 4.8 kHz respectively. Each of the three pulse trains is fed into a common-emitter saturating amplifier which provides some amplification and isolation. These outputs can be considered a by-product of the inverter since they are not needed to perform the inverter's basic function of converting unregulated dc to regulated 3ϕ ac.

The 4.8-kHz output of the ÷2 toggle flip-flop is, however, used elsewhere in the inverter. It determines the switching repetition rate of the switching regulator, and also is the "clock" for the six-flip-flop Johnson Counter shift register. The Johnson Counter is effectively a ÷12 circuit, as the output from each flip-flop in the register is 400 Hz.

The unique feature of the six-stage Johnson Counter is that each output signal is shifted 360°/6 or 30° in phase from the output of the preceding flip-flop. The 12 Johnson Counter outputs are connected to the push-pull darlington transistors which in turn drive the power transformers. The transformers' secondaries are connected in such fashion that the summed square waves form the low-distortion step-approximated 3ϕ sine waves.

The step-approximated sine waveshapes are then filtered by a 3ϕ low pass filter to obtain the low-distortion output from the three output terminals. Current and voltage sense transformers are also used to sample the line current and voltage of each phase. These sense signals, F(v) and F(i), are fed back to the switching regulator for voltage or current control of the inverter.

A controlled dc-voltage output from the switching regulator is supplied to the push-pull darlingtons and transformer combination. The magnitude of this voltage determines the magnitude of the ac square waves and hence that of the ac-output waveform. The ac-output voltage must remain constant from no load to full load, even though internal voltage drops in the basic inverter will vary with load. The dc output from the switching regulator must be capable of compensating for these variable internal voltage drops.

The dc-output voltage from the switching regulator is obtained by using the switching regulator to convert the unregulated dc input into a constant-frequency (4.8 kHz), variable-duty cycle power pulse train which is then filtered back to dc. With this approach the output dc can be made variable by controlling the duty cycle, which is varied by use of low-level circuitry comparing the appropriate sense signal F(v) or F(i) to an internally generated reference voltage. The resulting error voltage varies the switching regulator duty cycle and hence output dc voltage in such manner as to reduce the error voltage to zero. Thus the ac output is held to constant voltage or constant current (whichever is appropriate for the output load applied).

Current and voltage sense transformers provide voltages which are converted to a dc voltage proportional to the ac signals they represent. F(i) is made proportional to the peak value of ac output current. F(v) is proportional to the 3ϕ full-wave rectified average value of ac output voltage. Both signals are fed into a linear OR circuit, with output proportional to the larger of the two inputs.

This output is the control signal which is compared to a reference voltage by means of a differential amplifier. The differential-amplifier output is the error voltage determining the duty cycle pulse width. The inverter has been designed for maximum output of 150 percent rated load, or 113 VA, corresponding to output voltage of 26 V rms and output current of 2.5 A rms.

If the load impedance can sustain 26 V rms without drawing a peak value of line current of $2.5\sqrt{2}$ then the inverter will operate in the voltage mode and hold the output voltage constant at 26 V rms. If, however, in an attempt to sustain 26 V rms output voltage the peak value of line current does reach $2.5\sqrt{2}$ then the output voltage will adjust itself as necessary to hold this current constant since the inverter will be in the "current" mode.

The inverter has been designed to operate with any kind of balanced or unbalanced resistive or inductive (P.F. $\geq$ 0.5) load, including 3ϕ and 1ϕ short circuits.

B. HISTORY

This section is a brief review of the evolution of the inverter's circuit design. The contract was awarded on April 27, 1965. Progress reports were provided monthly, and a detailed subassembly-design report was submitted in March of 1966.

In July 1966 a breadboard was delivered; in December of 1966 the first production-model inverter was shipped to NASA. In April 1967 the final two production-model inverters were delivered.

Doubtless the most troublesome item encountered during development of the complete inverter system was the Johnson Counter. Regardless of whether the Johnson Counter comprised I/C flip-flops or discrete component flip-flops, prevention of malfunctions was difficult; usually they occurred at high ambient temperatures, high J. C. supply voltage, and high power output from the inverter. Through many modifications, proper circuit operation under all conditions was finally achieved. Another problem confronting early breadboards was low-frequency oscillations under certain conditions of loading. Proper shaping of the open-loop frequency response finally eliminated the oscillation.

The first breadboard was also designed to shut off when an overload was sensed and to cycle on and off until the overload was removed. Although this technique did protect the inverter during overloads, it was deemed less desirable than a current-limited overload mode. Consequently the breadboard was modified to provide the more desirable constant-current output during overload. In addition to being a better approach, this modification actually was achieved with simpler circuitry.

More often than not, unexpected and undesirable performance characteristics arise in a circuit whenever the physical layout is revised. For this reason considerable care was taken to build the final breadboards as much like the proposed production model as possible. As a result there was good correlation between final-breadboard and final-production-model performance.

C. DETAILED CIRCUIT DESCRIPTION

Figure 7, the combination schematic and wiring diagram of the inverter, will be referred to frequently in the following more detailed discussion of the inverter's various subassemblies. The associated parts list is given in Appendix B.

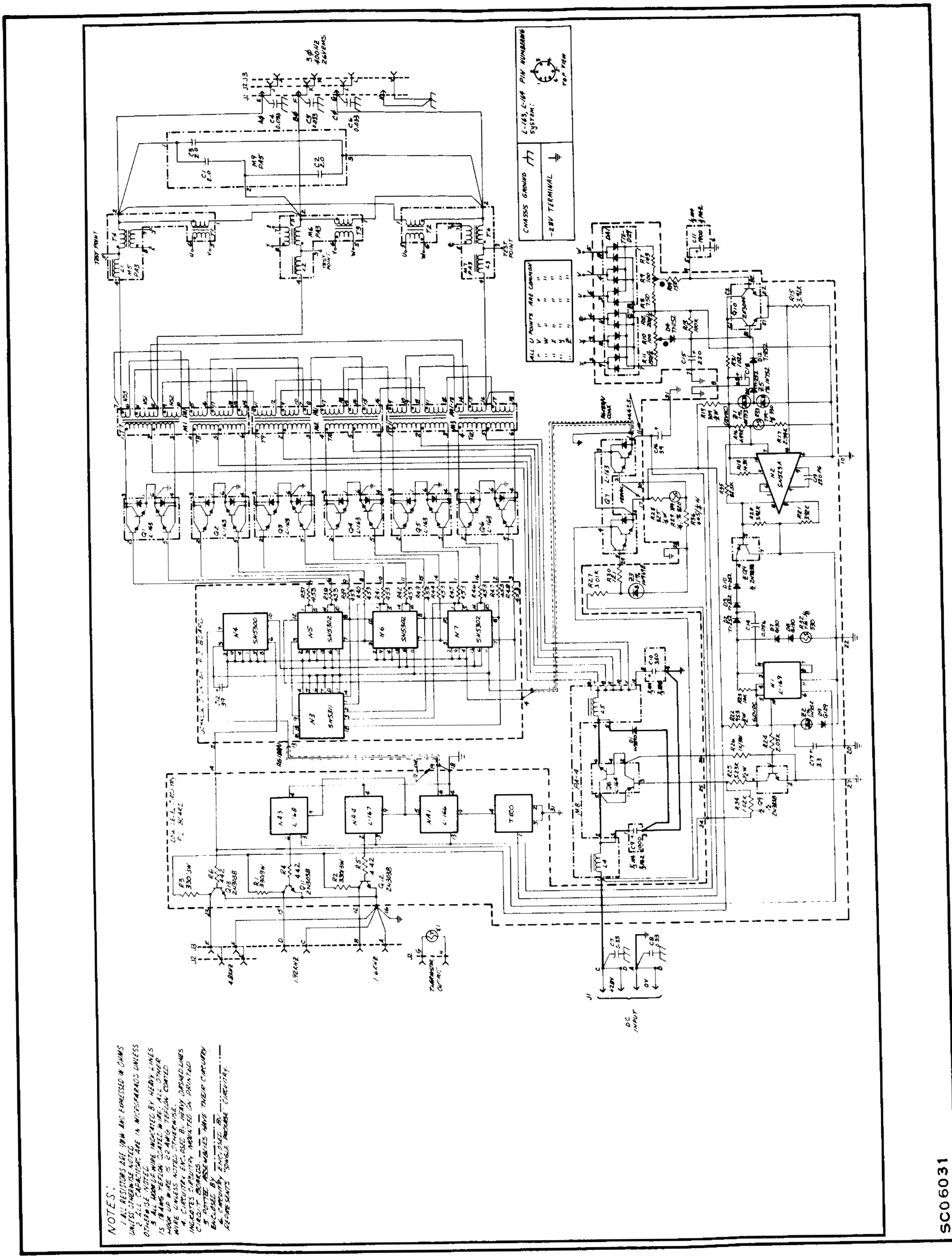


Figure 7. 75 VA Static Inverter — Model A — Schematic and Wiring Diagram

1. Subassemblies

a. TXCO and Associated Countdown Circuitry

The temperature-compensated crystal oscillator (TXCO) draws approximately 10 mA at 12 V dc. Output is a 2.4576-MHz, 50-percent duty cycle pulse train (see Figure 8 for loaded output waveform). The TXCO acts as the inverter "clock," as all outputs are derived from its 2.4576-MHz output. The ÷10, ÷12, and ÷256 I/C arrays (NA3, NA4, and NA1 respectively) are simple frequency dividers. They and the TXCO are discussed in further detail later.

b. Johnson Counter Printed Circuit Board

The components on the Johnson Counter P.C. board are a power-supply decoupling capacitor C12; twelve isolation resistors R37-R48; a clock driver

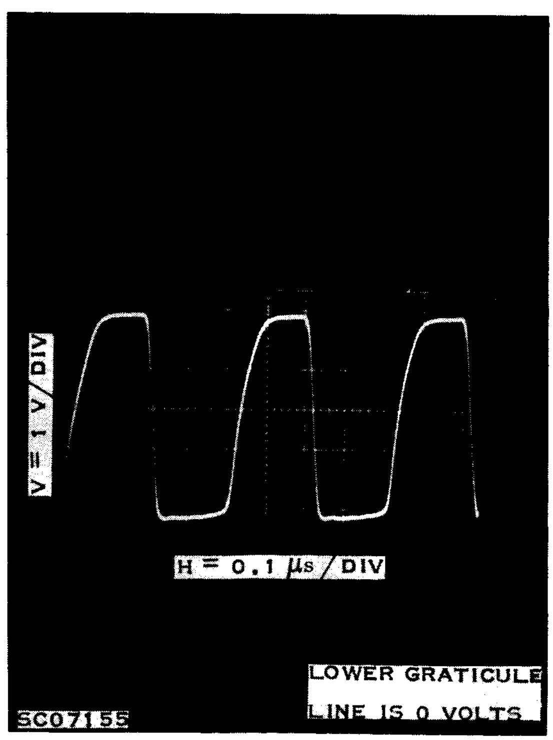


Figure 8. Output Waveform of TXCO

(÷2 toggle flip-flop N4); and the dual flip-flops (N5, N6 and N7) and the NAND gate (N3) which comprise the basic Johnson Counter. N3 provides the capability of restoring the flip-flop outputs to the correct sequence within at least five clock pulses if an illegitimate count sequence should occur at any time.

The resistors are necessary to provide a degree of isolation between the two loads of a particular flip-flop output. One load is the base-emitter diodes of the darlington transistor; the other is the logic input of the next flip-flop in the Johnson Counter. During portions of the ON time of a darlington transistor the rectifier shunting collector emitter becomes forward biased. During the time this diode is forward biased the V_{BE} voltage (normally at approximately 1.5 volts) drops to a voltage of -0.1 V or -0.2 V. The 453-ohm resistors help isolate the logic load from this variation in V_{BE} load.

Coaxial cable was used on the power-supply line and also on the 9.6-kHz pulse train input to N4 because of problems experienced during breadboard evaluation of the system. Noise caused by the power section of the switching regulator could cause a malfunction of the Johnson Counter. A combination of careful grounding and routing of wiring and the use of the coaxial cable was necessary to eliminate the problem in the breadboard, and consequently the same techniques were applied to the final systems.

c. Power Transformers and Darlington Transistors

Collector current and collector-emitter voltage waveforms of the darlington transistors for various types of loads are seen in Figures 9 and 10 respectively. The waveforms are effectively identical for all transistors except for conditions of unbalanced 3ϕ loading.

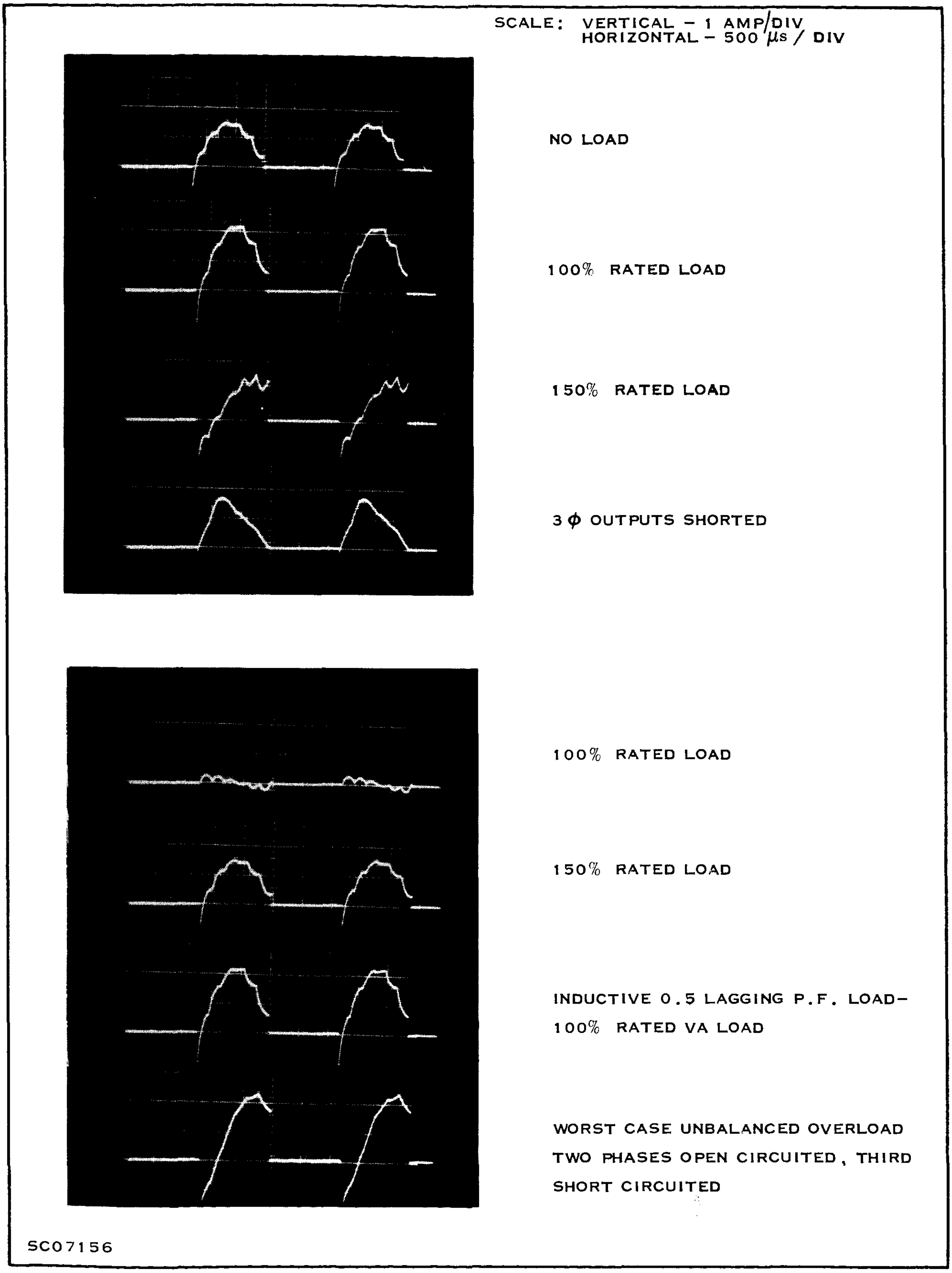
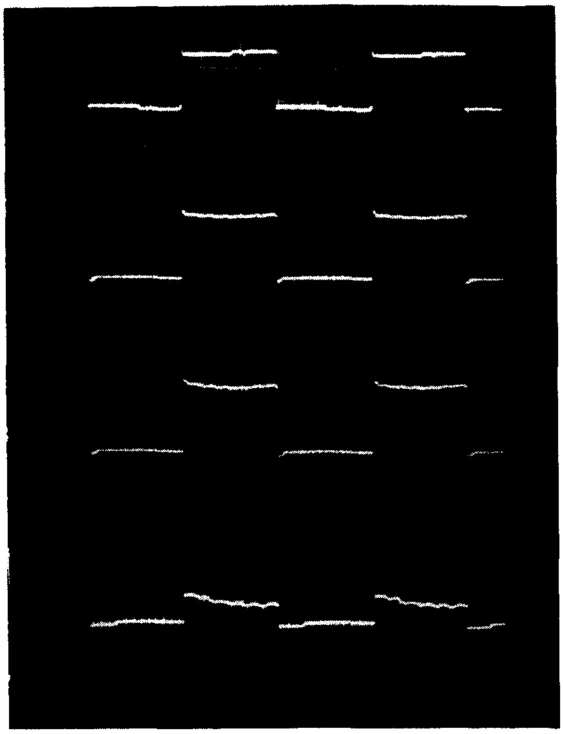


Figure 9. Power Darlington Collector — Current Waveshapes

NOTE: A 20 V 2 μs SPIKE NOT BRIGHT ENOUGH TO BE SEEN IN PHOTOS EXISTS ON LEADING EDGE OF EACH WAVEFORM SHOWN BELOW.



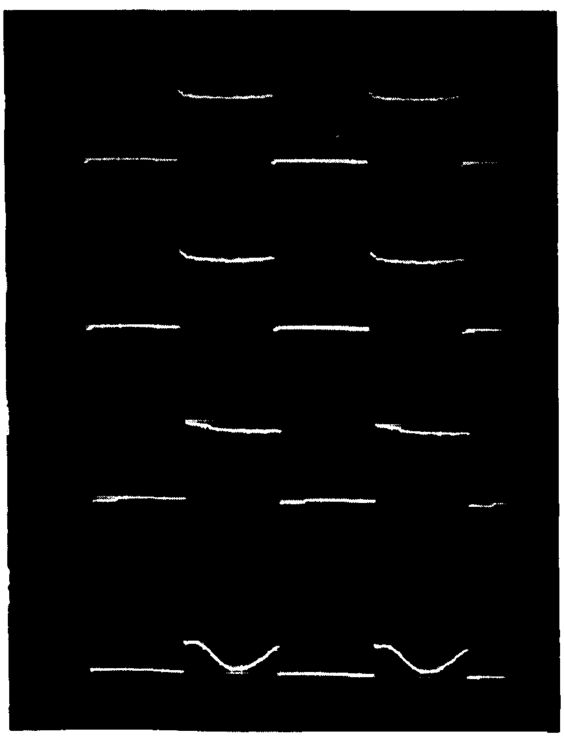
NO LOAD

100% RATED LOAD

150% RATED LOAD

3ϕ OUTPUTS SHORTED

SCALE: VERTICAL – 20 V/DIV
HORIZONTAL – 500 μs/DIV



100% RATED LOAD

150% RATED LOAD

INDUCTIVE LOAD; 0.5 LAGGING P.F.– 100% RATED VA LOAD

WORST CASE UNBALANCED OVERLOAD, TWO PHASES OPEN CIRCUITED, THIRD SHORT CIRCUITED

SC07157

Figure 10. Power Darlington Collector — Emitter Voltage — Waveshapes

Peak collector current which occurs for any type of loading is shown by the 2.5-A peaks in Figure 9 for the 3ϕ short. The negative spikes of current represent the current flowing through the rectifier shunting the collector-emitter terminals of the darlington. This rectifier becomes forward biased because of the induced emf caused by the reactive loading applied to the transformer secondary. Even with a 3ϕ resistive load applied to the output terminals the 3ϕ low-pass filter represents a noticeable reactive load as evidenced by the negative excursions of current noted in Figure 9.

The collector to emitter voltage waveshapes presented in Figure 10 reveal a maximum repetitive voltage of approximately 60 volts, including the 20-volt leading-edge spike referred to in the note on Figure 10. The spike voltage is attributed to leakage inductance remaining in the transformer primaries despite the fact that they were bifilar wound.

The current and voltage waveshapes seen in Figures 9 and 10 are representative of the worst-case repetitive conditions to which the darlingtons are subjected. However, during initial turn-on of the inverter a transient condition subjects the darlington to slightly greater peak voltages and currents.

Detailed information on the potted assembly of power transformers (along with information on all other potted assemblies) is presented in the Supplement, Exhibit D. The cores are tape-wound toroids with a rectangular hysteretic B-H characteristic; but the design assures that, even with maximum possible transient voltage applied to the transformers, the cores will not saturate. The secondary turns were chosen to provide proper-magnitude square waves for the desired step-approximated wave shape.

d. 3ϕ Filter, Current, and Voltage Sense Transformers

The step-approximated waveform before filtering has the 11th as the first existing harmonic. Consequently, the filter was required to pass 400 Hz but attenuate 4.4 kHz. Break frequency of the filter is designed to occur at approximately 2 kHz. The slight variation in output waveshape distortion occurring with various loads is probably caused in part by the shifting break-point frequency, since the value of filter inductance is not independent of load current at higher output loads.

Secondaries of the current sense transformer are tied in a delta, as are the secondaries of the voltage sense transformers. The resulting 3ϕ voltages are then full-wave rectified by the TIXD29 diode array (DA1).

e. Low-level Switching-regulator Circuitry

The two dc voltages obtained as outputs from DA1 have their magnitudes reduced by a resistor voltage divider, and then each is filtered to reduce ripple. The voltage proportional dc signal is filtered by a low-pass R-C filter while the current proportional dc signal is fed to a simple peak detector circuit (D4, R13, and C15). Voltage at pin B1 of Q10 is then a dc level proportionate to the peak value of ac line current; voltage at pin B1 of Q10 is a dc level proportionate to the rectified average value of ac output voltage.

Q10 acts like a linear OR circuit, with voltage at E1 and E2 proportionate to the largest magnitude base signal. The trimpots R10 and R9 are adjusted to achieve "crossover" from constant voltage regulation to constant current regulation whenever the output current is increased to 2.5 amps (150 percent load).

Control voltage from the emitters of Q10 is fed to one of the differential inputs (pin 14) of N2. The other input (pin 7) is a dc reference voltage from a resistor-divided zener voltage. The resistor voltage divider is temperature compensated by the sensistor R33.

The differential amplifier's frequency response is shaped by means of capacitor C13 and its gain controlled by the negative feedback resistor R35. The differential amplifier output is taken from pin 12. Output is dc voltage proportional to the amplitude error of the ac output signal. This error-voltage output is buffered by the use of one-half of Q9 as an emitter follower with the capability of sinking current. N1 and the rest of its associated circuitry located between both halves of Q9 in Figure 7 are a duty-cycle-modulated one shot. Details of circuit operation will be presented in a later section. In short, it operates in the following manner:

It has as input a 4.8-kHz 50-percent duty cycle square wave fed into pin 6 of N1. Its other input is the dc error voltage present at pin 4 of Q9. The output, taken from pin 10 of N1, is a 4.8-kHz varying duty cycle pulse train. The pulse width variation is proportionate to the magnitude of the dc error voltage. This varying duty cycle pulse train is amplified by the NPN portion of Q9 and both portions of Q8.

f. <u>High-level Switching-regulator Circuitry</u>

The filter (L4 and C9) connected to the dc input terminals attenuates unwanted electrical spikes entering or leaving the dc input terminals. Series switch Q8 of the switching regulator is controlled by the varying duty cycle pulse train discussed above. During the interval when Q8 is ON, the dc input voltage is effectively applied directly to pin 4 of M8; consequently the current flowing would be the required load current from the output pins (6 through 11) of M8 and the charging current for C10. The rectifier D1 would not be conducting during this period.

During the interval when Q8 is OFF, the induced voltage in L5 would cause D1 to be forward biased and current would flow through D1, L5, and the parallel combination of C10 and load (i.e., darlingtons). The OFF interval is sufficiently long so that for most conditions the induced current will decay to zero, and load current will then be supplied from the stored charge in the capacitor C10.

Output voltage of this switching regulator is the input voltage for the basic inverter, and consequently its magnitude determines the magnitude of the ac output signals. The dc voltage out of the switching regulator is approximately equal to $E_{IN}\tau$ where E_{IN} = dc input voltage and τ = duty cycle of pulse train.

In summary then the output ac signal error causes a particular τ. This value of τ in turn causes a particular value of ac output signal. The loop is closed and the inverter has its outputs regulated against input voltage variations as well as load variations.

Power supplies for the low-level circuitry are obtained by using the Q7 darlington as simple series regulators to obtain 20 V dc and 4.5 V dc. The 4.5-V dc supply uses a sensistor, R29, to vary the supply voltage with temperature. The 4.5-V dc is a typical room-temperature value, while at +125°C it decreases to about 4.0 V dc and at -25°C it increases to about 5.0 V dc. This temperature compensation was done for the benefit of the Johnson Counter, which proved to be sensitive to high values of V_{CC} at high ambient temperatures.

2. Trouble-shooting Procedure

Refer to the schematic and wiring diagram shown in Figure 7. With all power OFF, unsolder wire connected to pin 4 of M8. Turn power supply on. Loads for outputs are immaterial; any normal load may be used (e.g., no load, full load, overload, etc.). Normal outputs should be obtained from pulse train outputs only. Check to see if amplitude, frequency, and waveshape are correct. Typical unloaded outputs from pulse trains are seen in Figure 11. Then connect scope to unsoldered wire which is still connected to pin 6 of Q8. The correct waveshape would be one similar to that shown in Figure 12.

Next, turn off input supply and connect auxiliary dc supply between the bare pin 4 terminal of M8 and ground. Make sure the voltage adjust knob of this additional supply is at zero and then turn on both the input and auxiliary supplies. CAUTION: When turning off supplies always turn off auxiliary supply first and input supply second. Failure to do this could destroy some of the Q1 - Q6 darlingtons.

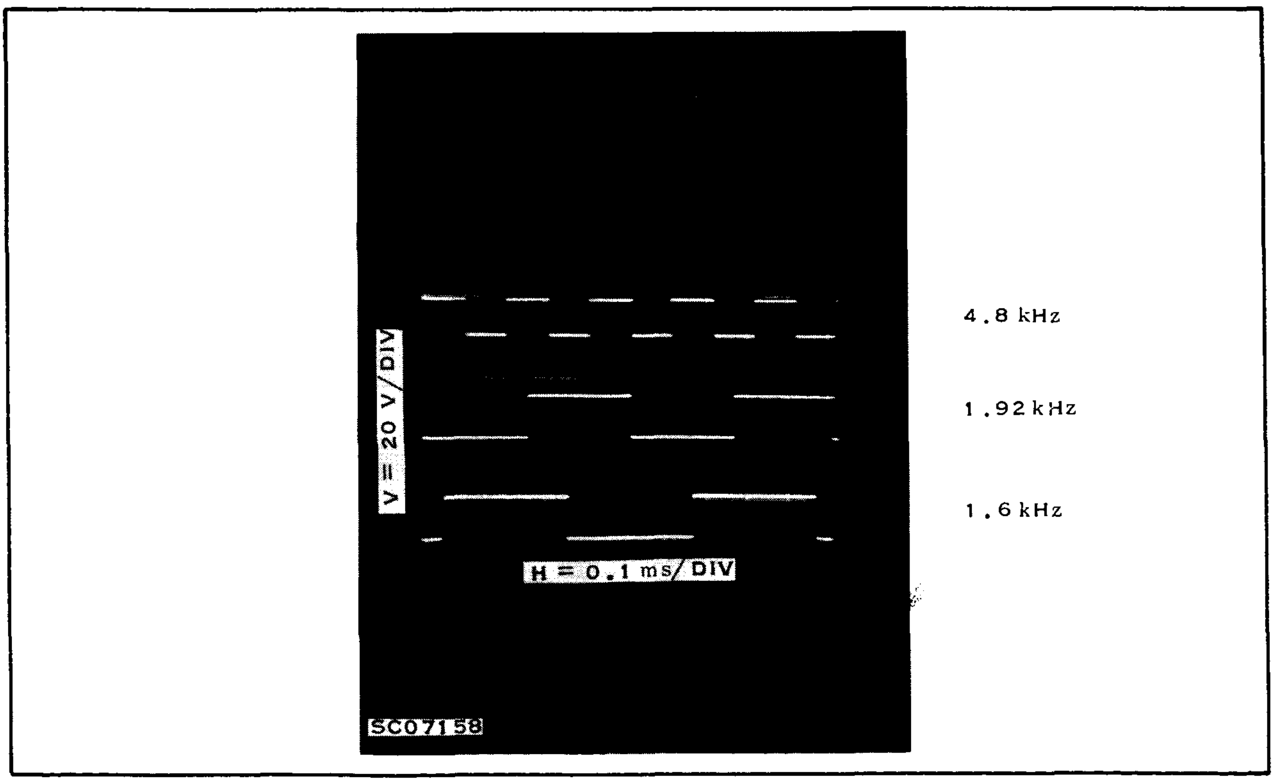


Figure 11. Pulse Train Outputs

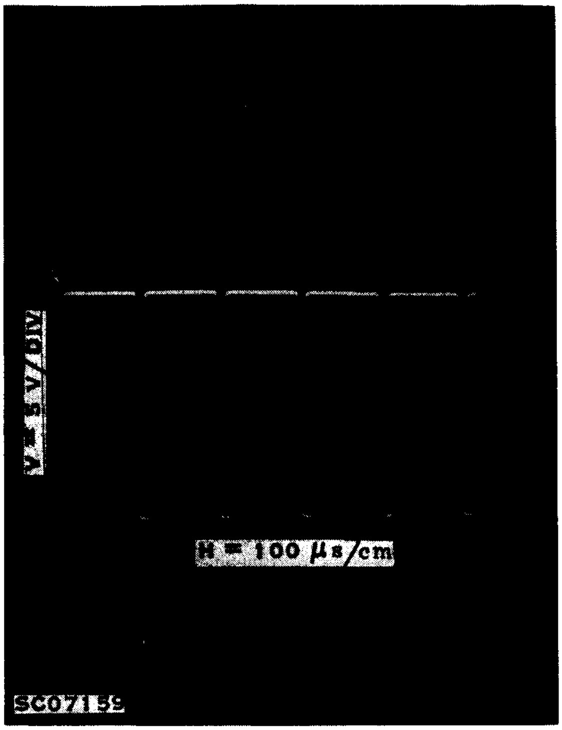


Figure 12. Waveshape at Pin 6 of Q8 (Figure 7)

Now, with both supplies ON but auxiliary supply at zero volts, increase output of auxiliary supply to several volts. Check output signal on 3ϕ outputs. Signal should be correct waveshape but reduced magnitude. If waveshape is correct, the dc output of the auxiliary supply can be increased until the proper 3ϕ ac output amplitude is obtained for the load applied.

Once the proper ac output amplitude is obtained, slight variations in the auxiliary dc supply will cause the duty cycle of the pulse train at pin 6 of Q8 to vary from 0 percent duty cycle to the maximum shown in Figure 12. A dummy load resistance can be applied to the emitter of Q8, even more closely to synthesize closed-loop operating conditions.

If the 3ϕ output waveshape is distorted upon application of several volts from the auxiliary supply, the problem could be a malfunction of the Johnson Counter or a bad darlington, Q1 to Q6. With several volts out of the auxiliary supply the output of the Johnson Counter can be probed with a scope. Collector-emitter voltages of the darlingtons can also be probed. Probing at the primary terminals of the power transformer is most convenient.

To help with trouble-shooting, the physical locations of the components referred to in Figure 7 are identified as follows: Figure 13 gives the location in the inverter housing of all components not located on printed circuit boards.

Figures 14 and 15 show the Johnson Counter printed circuit board and the low-level circuitry P.C. board respectively. Note that the P.C. board terminal numbers referred to in Figure 7 are also identified in these figures.

3. Electrical Testing and Performance Data

a. Dummy Loads

In order to accurately evaluate inverter performance, a load box was fabricated from precision resistors and arbitrarily wired in a delta configuration. The following discrete values of load resistance were built into the box:

ΔR_L	% Full Load Power Calculated	
∞	0	(No Load)
270	10	
150	18	
100	27	
54	50	
27	100	(Full Load)
18	150	(Current-voltage Mode Crossover Point)
16	132.5	
14	115	
10	84	
5	41.5	
0	0	(3Φ Short)

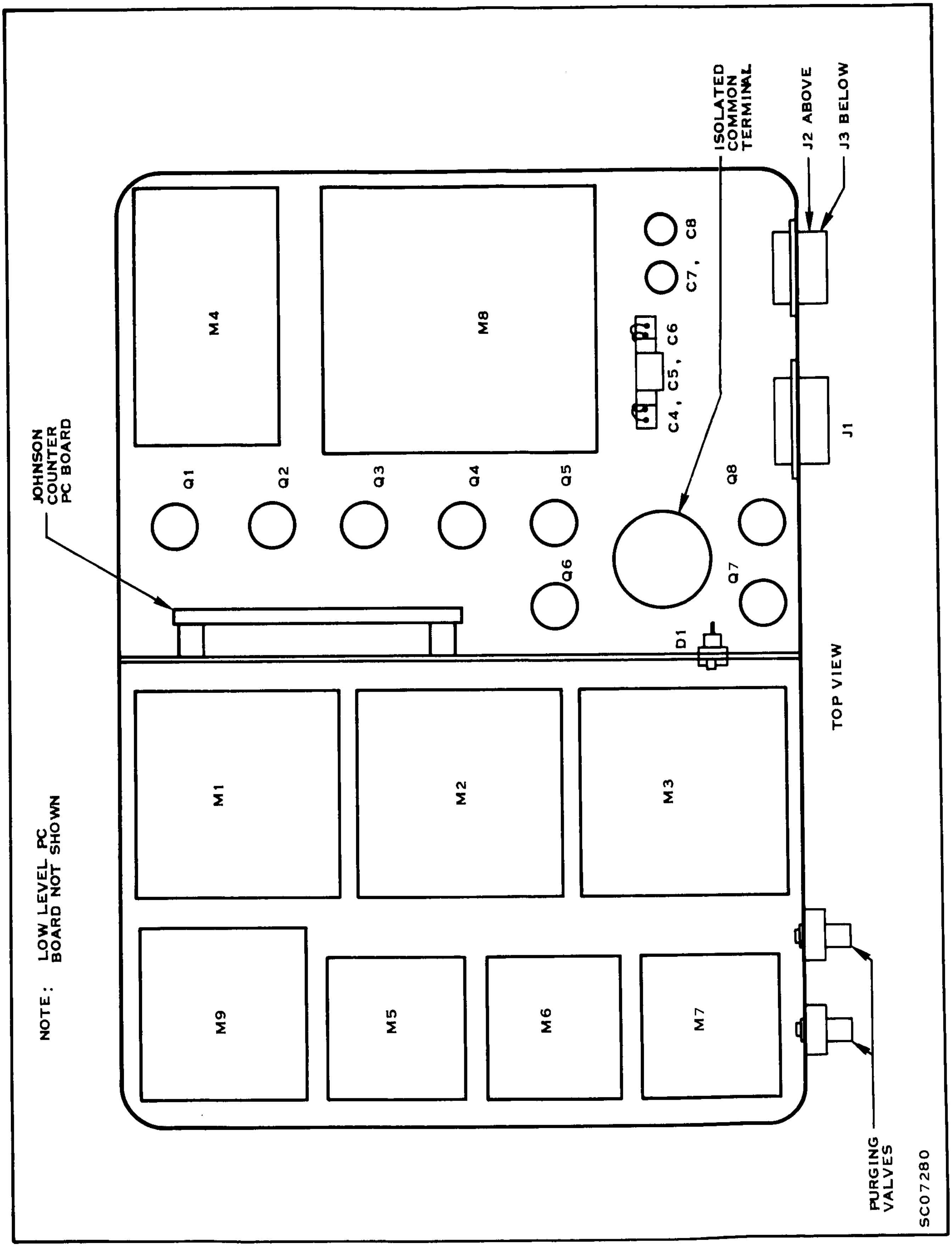
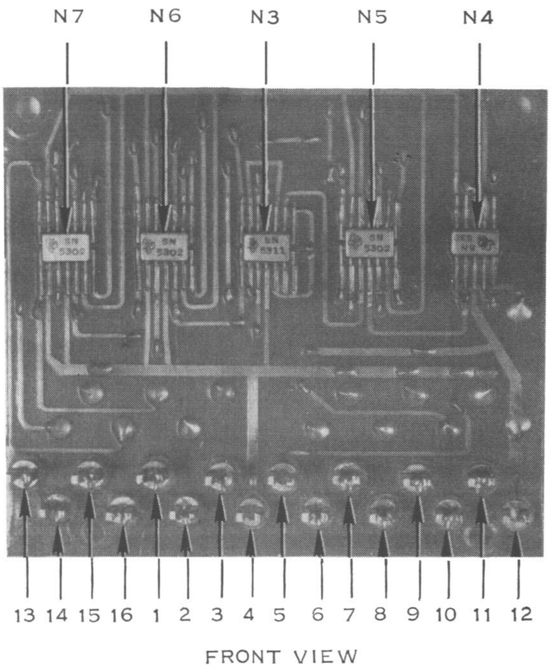


Figure 13. Component Locations in Inverter



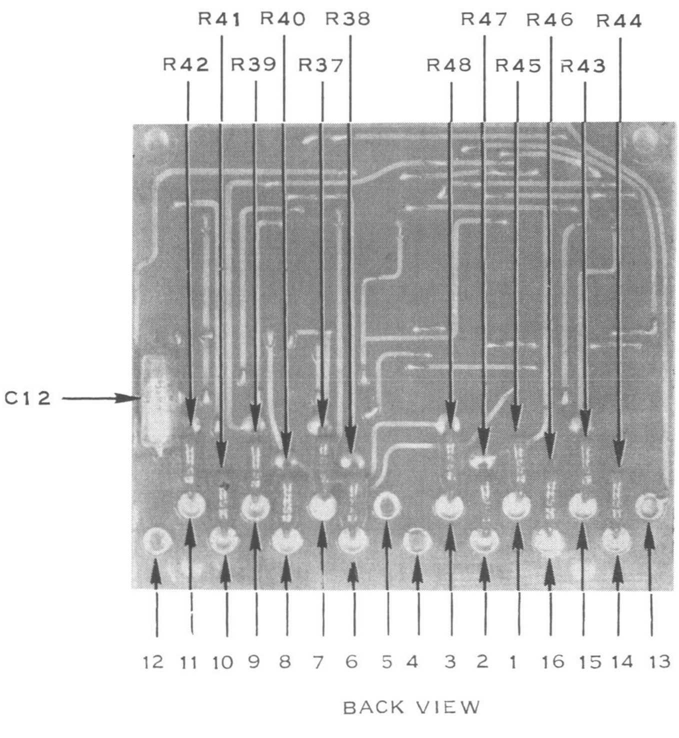


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Figure 14. Johnson Counter Printed Circuit Board

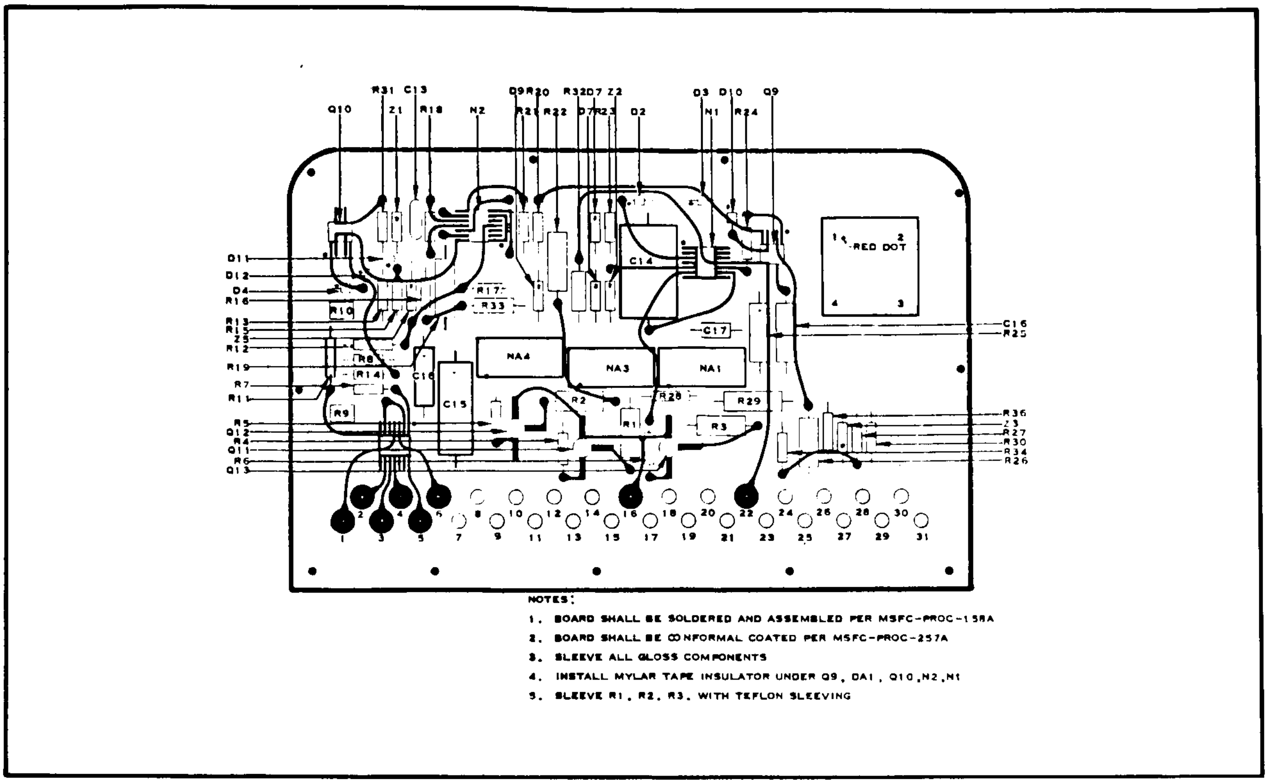

Figure 15. Low-level Circuitry Printed Circuit Board

The load box was so designed that all three-phase resistors could be varied at the same time to permit changes of load in a balanced condition, or the load resistance for each phase could be varied individually.

In order to evaluate inverter performance with an inductive load, a load which represented 100 percent load with a lagging 0.5 P.F. was built. Its electrical schematic is seen in Figure 16.

A continuously variable load was also used for testing inverter performance. A variable autotransformer was used to provide the variable load as shown in Figure 17. The dummy load for the three pulse-train outputs was arbitrarily chosen to be a 1K load resistor for each output.

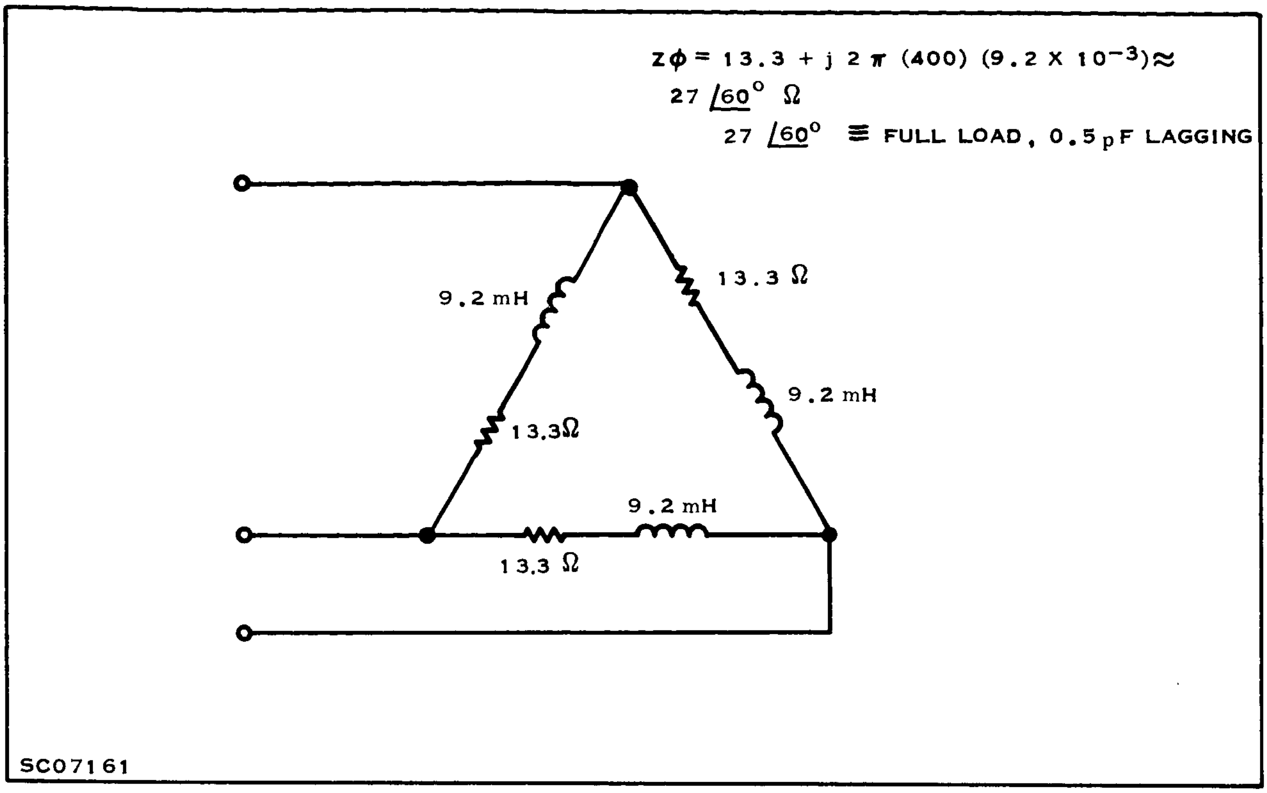

Figure 16. Inductive Load

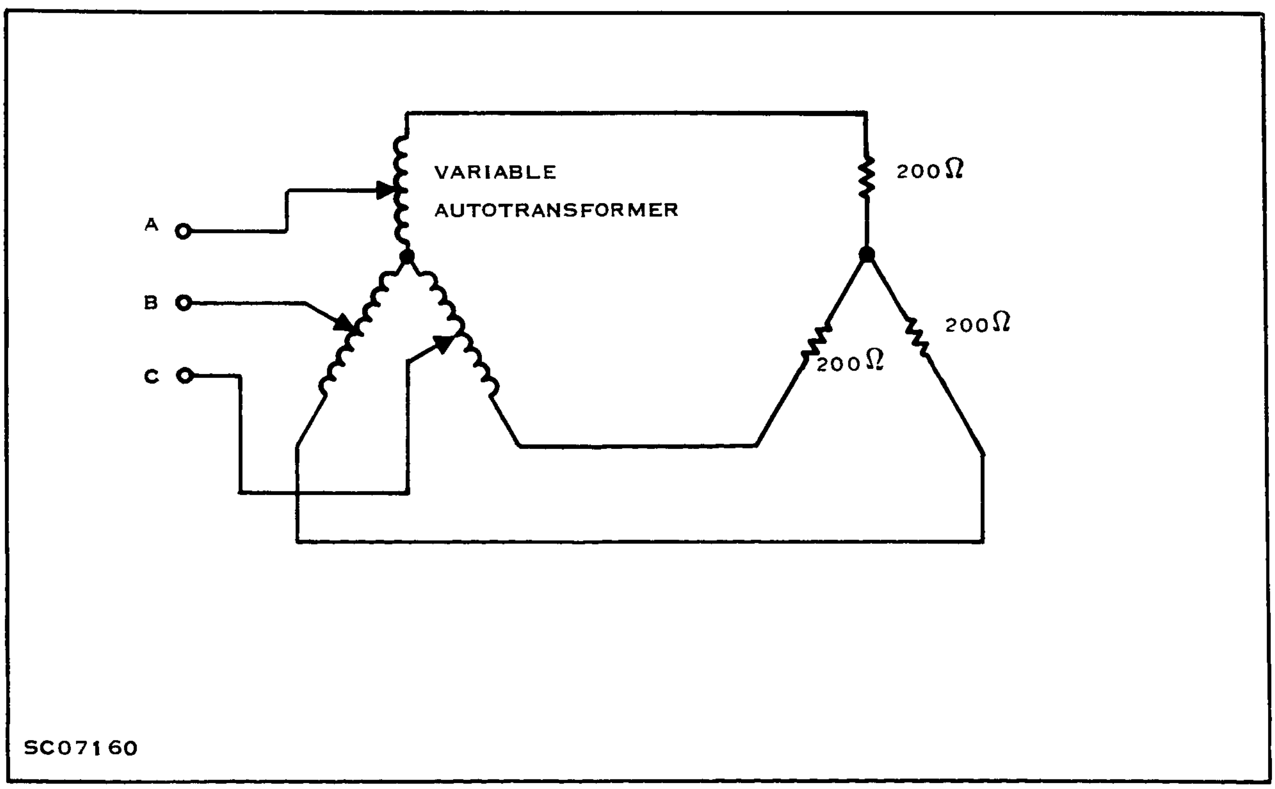

Figure 17. Continuously Variable Load

b. Test Procedures

Of the four production-model inverters built, two (NASA's #1001 and TI's #1002) were temperature tested from -25°C to +125°C, while the other two (NASA's #1003 and #1004) were tested only from -25°C to +50°C. With the exception of this difference in temperature testing, all four inverters were subjected to identical evaluation tests. This evaluation test consisted of data points taken on the regulation of output voltage as a function of load, input voltage, and ambient temperature. In addition various operational tests were performed with different loads while monitoring the outputs with an oscilloscope. These observation tests were made at 28, 25, and 30 V dc input at room temperature and the high- and low-temperature extremes.

c. Performance Data

The 3Φ ac output waveshapes before and after filtering are seen in Figures 18 and 19. Distortion of the filtered waveshape is only slightly above 3 percent when measured with an HP 330B distortion analyzer. (NOTE: An HP 3400A rms meter was used as the meter indicator for this test instead of the meter built into the distortion analyzer.) The effect of load variations upon the output waveform distortion is shown in Figure 20.

Inverter performance can be evaluated fairly easily by observing output waveshapes for various types of balanced and unbalanced loads. The waveforms shown in Figure 21 represent typical output waveform for a variety of load conditions.

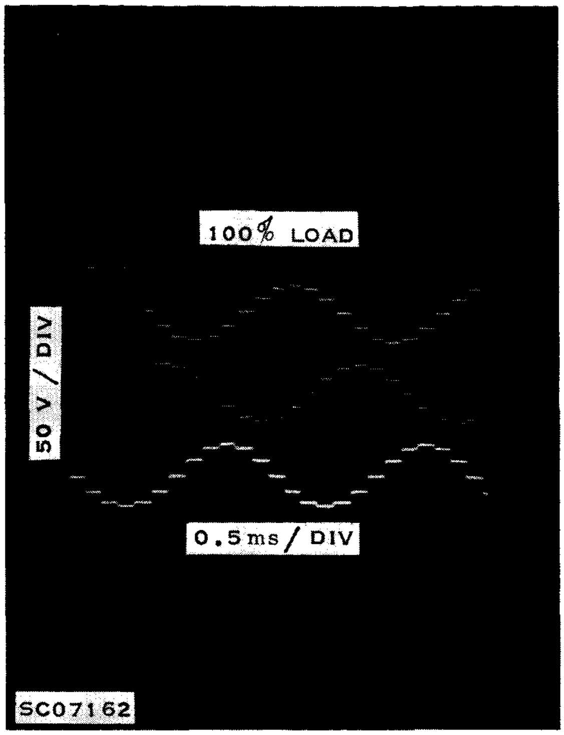

Figure 18. Unfiltered 3Φ Output

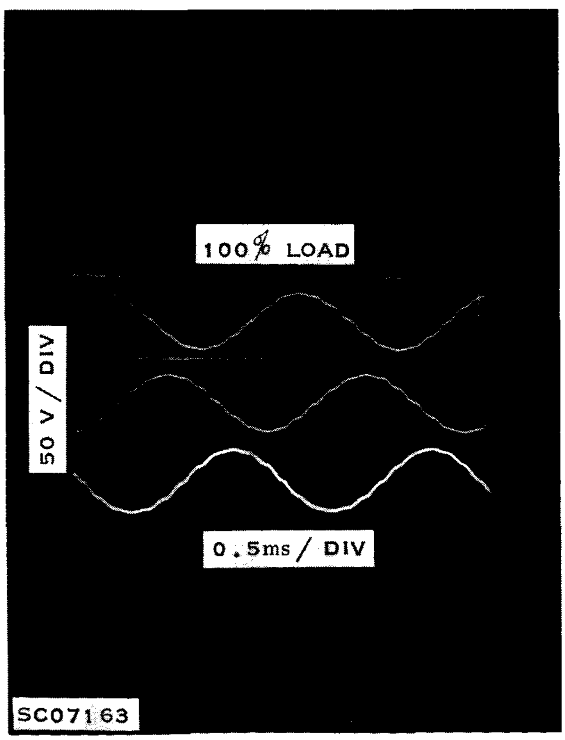

Figure 19. 3Φ ac Output

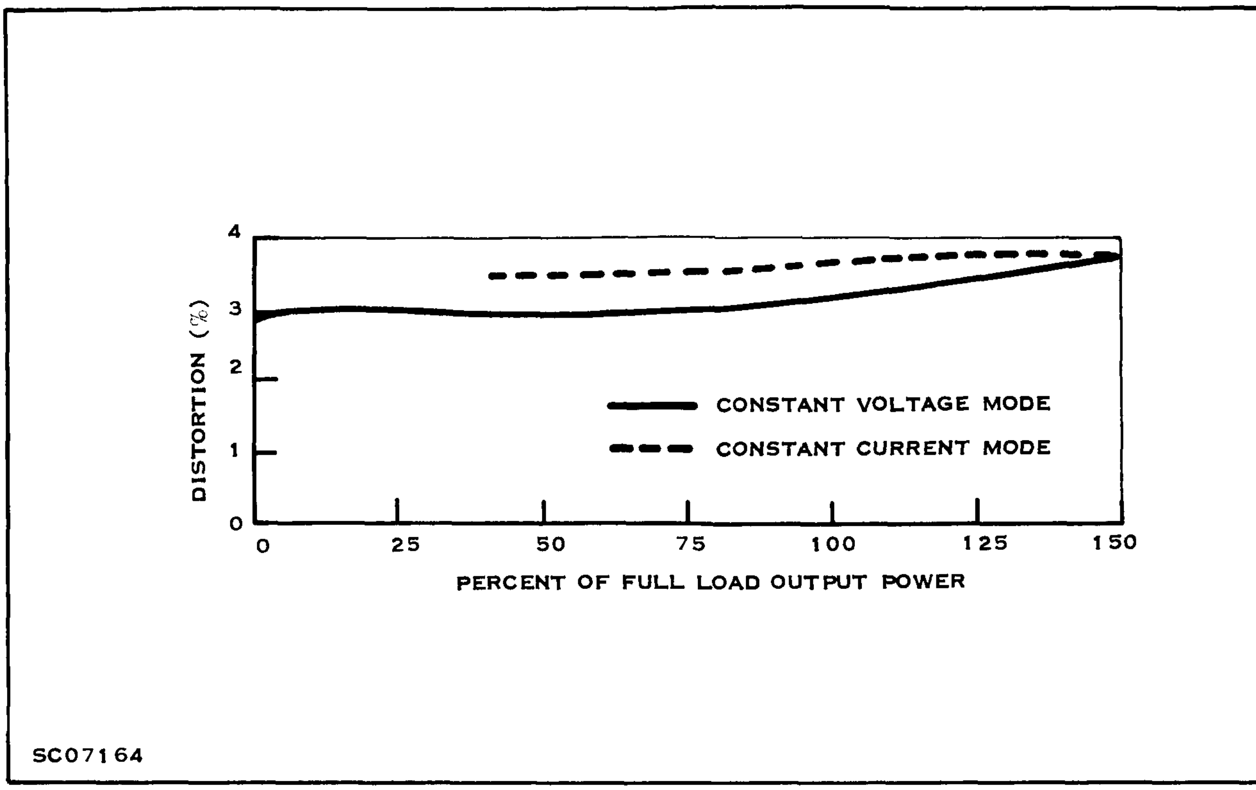

Figure 20. Output Waveform Distortion

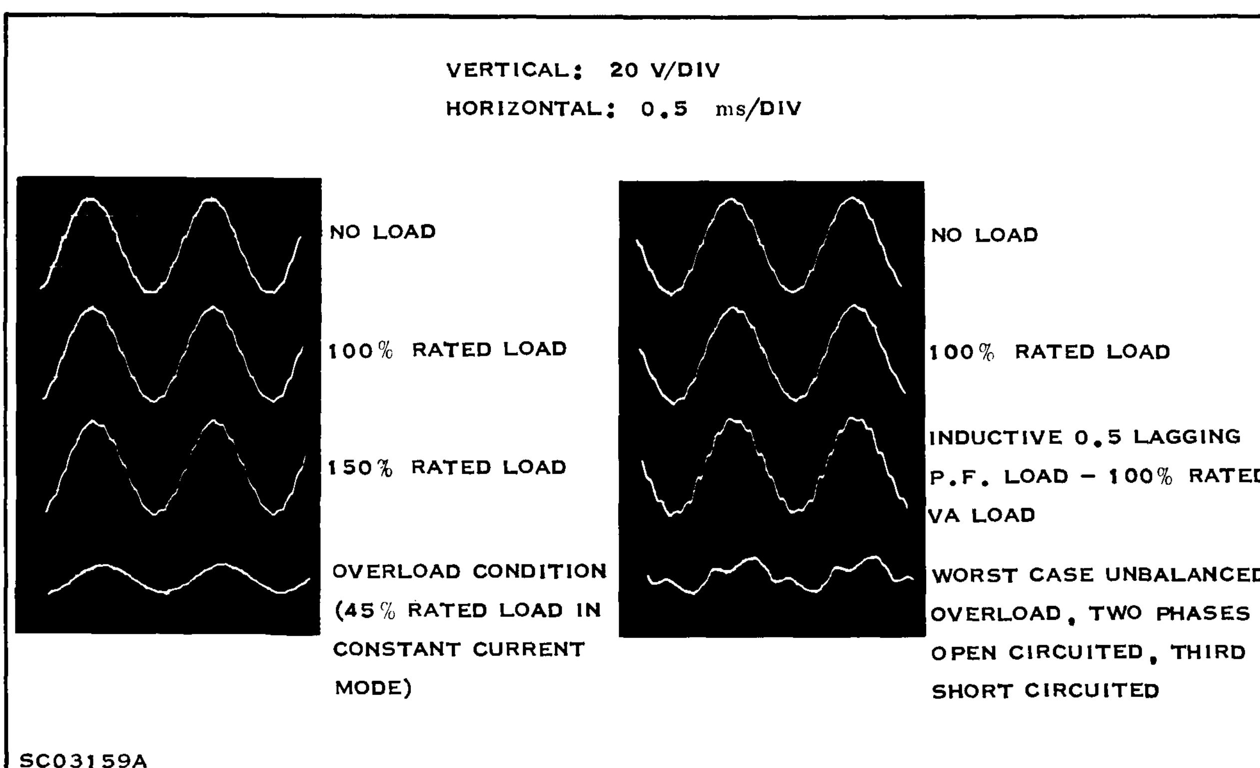

Figure 21. Output Waveforms

The fact that the inverter output is regulated to furnish a constant-voltage output for all loads up to 150 percent full load, and then to provide constant-current regulation when in the "overload" mode, is an important feature of the unit. The constant-voltage constant-current output characteristic plotted in Figure 22 is a graphical record of this self-protective feature.

The inverter's efficiency as a function of 3Φ ac output power is shown in Figure 23. Notice that the fixed power loss at no load is approximately 16 watts, and maximum power loss at 150 percent load is approximately 58 watts. The overall efficiency at full load is approximately 67 percent.

The 3Φ ac output was designed to be maintained at constant voltage independent of load variations from no load to full load, and input dc voltage variations from 25 to 30 V dc and from ambient temperature variations of -25°C to +125°C. The

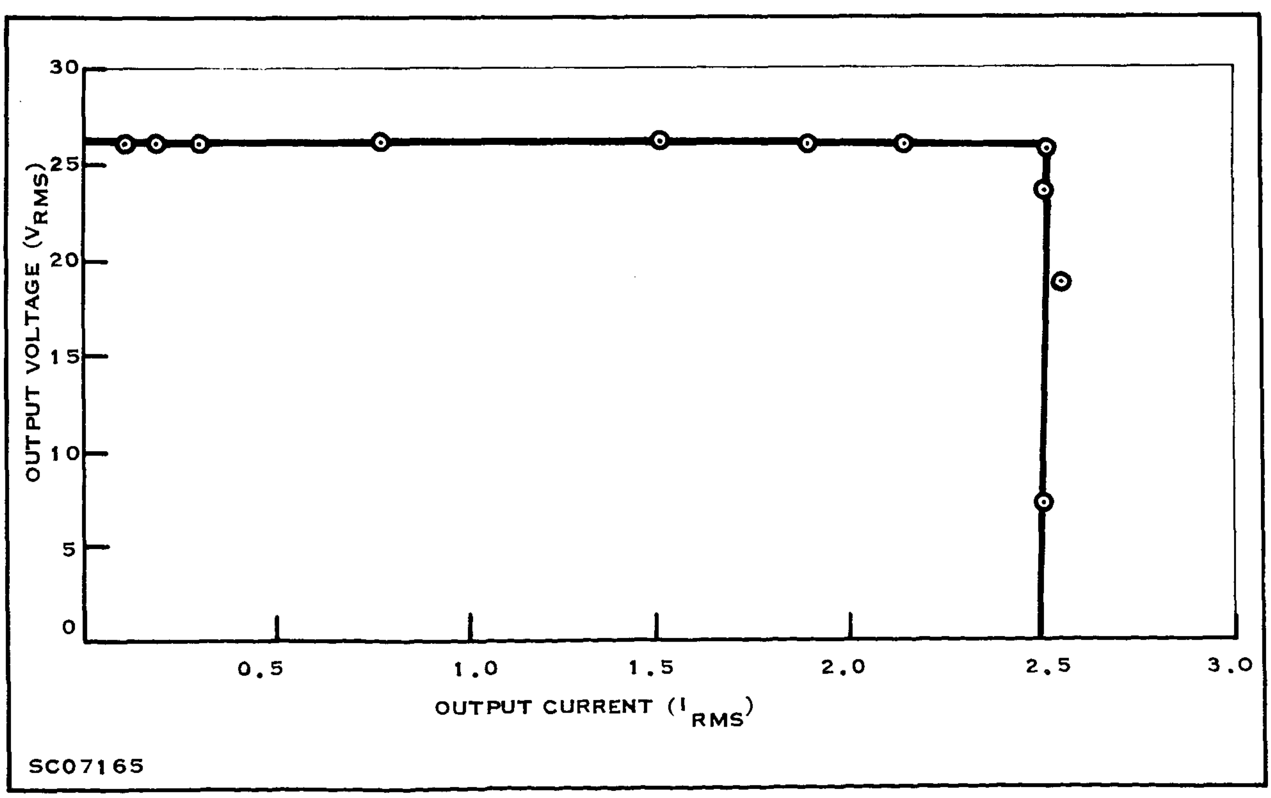

Figure 22. Output Voltage-current Relationship

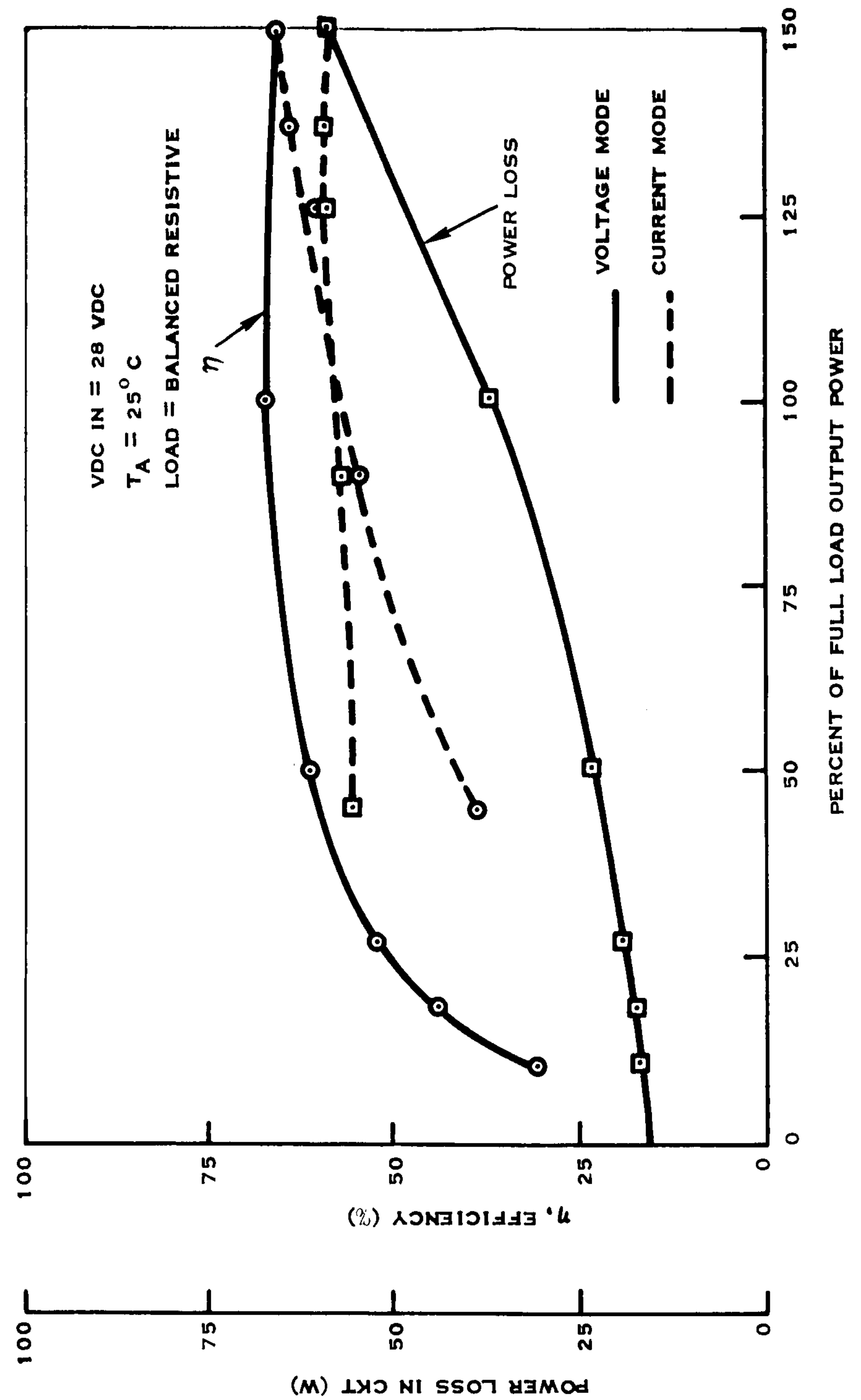

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Figure 23. Inverter Efficiency

curves seen in Figures 24 and 25 reveal the actual effects of these variables upon the voltage regulation.

Actual data from which most of these curves were plotted are given in Appendix C. More details — such as the fact that in none of the inverters did the voltage of a single phase ever differ from the other phases by more than a tenth of a volt (assuming a balanced load) — can be obtained from a study of these data.

d. Recommendations

Since the electrical performance of the inverter actually exceeds the original specifications we have no recommendations as to refinements which could improve the performance characteristics of future inverters of this type. However, with respect to inverter reliability it is true that each succeeding design can be

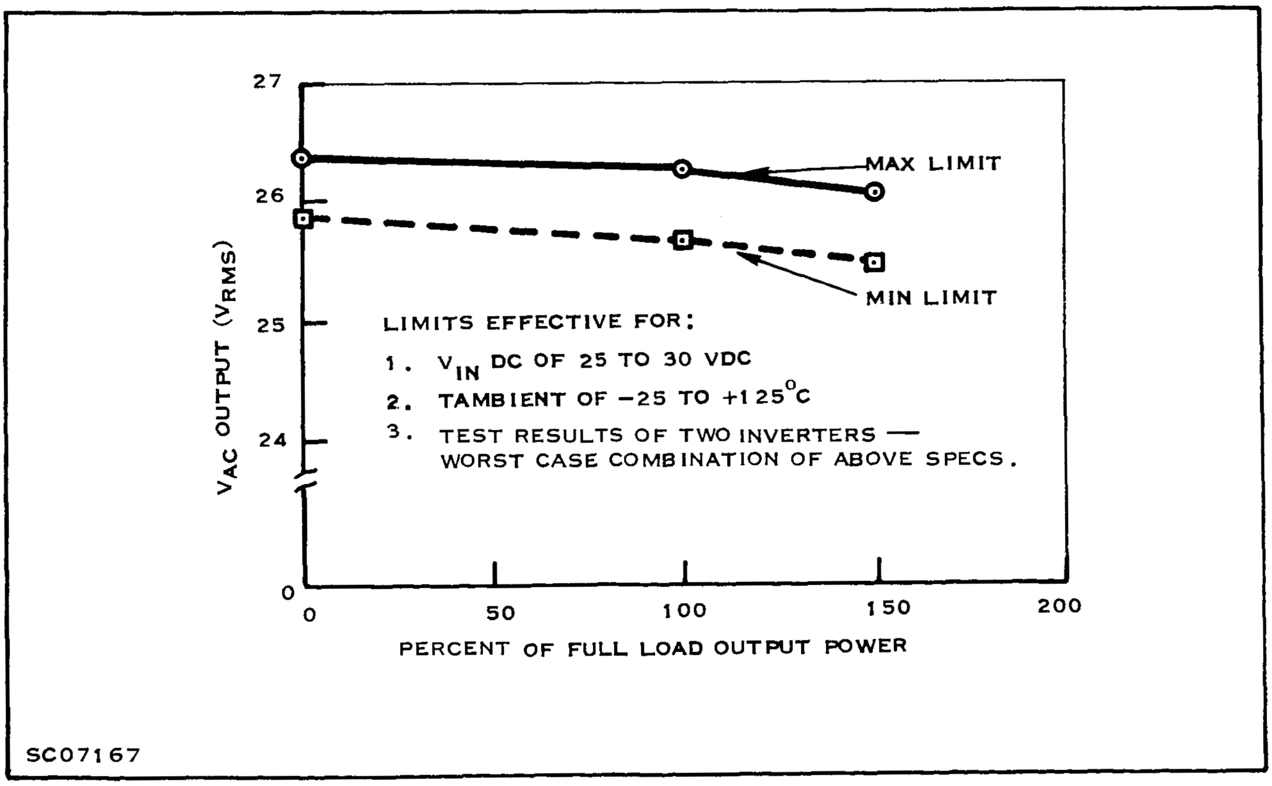


Figure 24. Voltage Regulation Limits

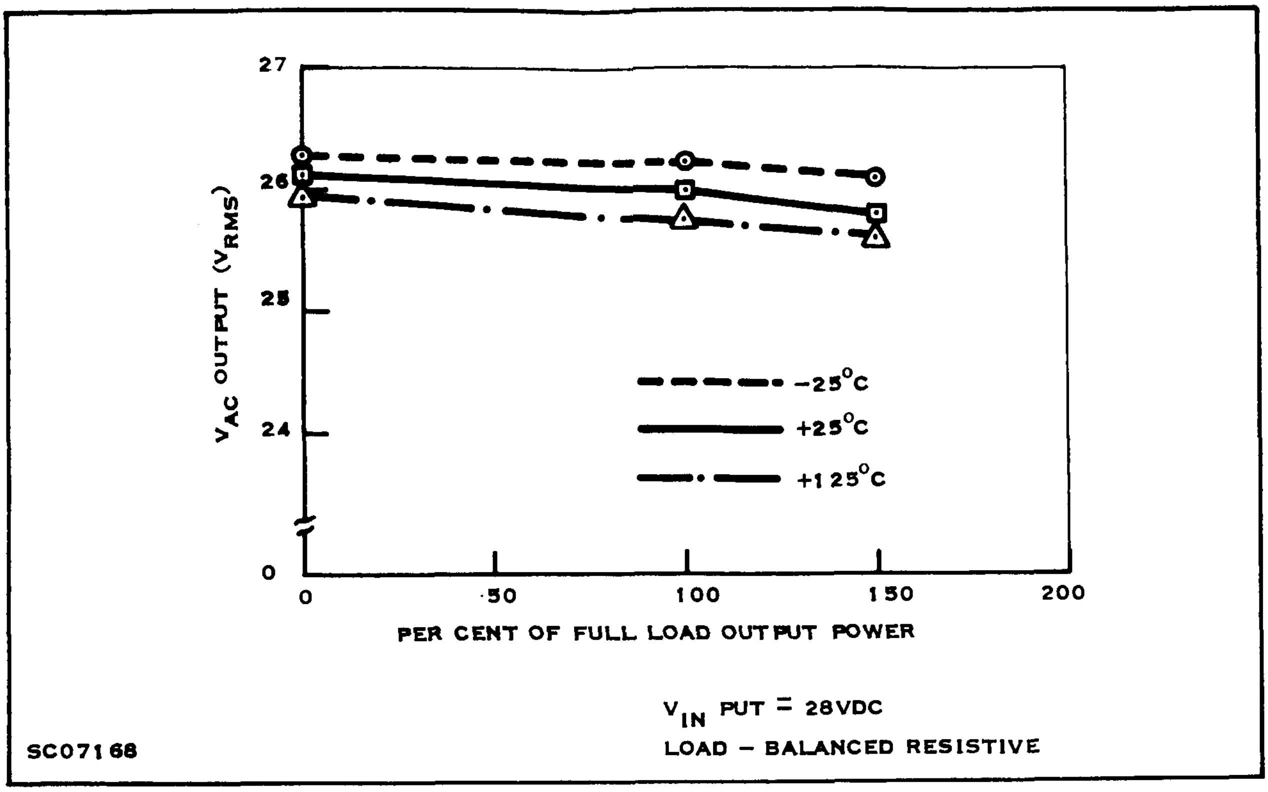


Figure 25. Load and Ambient Temperature Effects Upon Voltage Regulation

improved to provide a greater margin of safety. Several recommendations should be considered in a future redesign.

The two trimpots used in the low-level-circuitry portion of the switching regulator could be replaced with fixed resistors of selected values. Instead of having the Johnson Counter circuitry and all flip-flop arrays sharing one low-level regulated supply, it would seem to be more advantageous for the Johnson Counter to have its own separate supply.

Also, the 20-volt supply for the three-pulse train outputs should be a completely separate supply instead of an integral part of the complete low-level supply system as at present. This would prevent an accidental short on the pulse train outputs from affecting the 3ϕ ac outputs.

An additional safety margin could be achieved by using 75 or 80 V BV_{CEO} darlingtons in the Q1 - Q6 positions (see Figure 7) instead of the 70 V BV_{CEO} used now. However, in order to attain this higher breakdown the low-temperature specification on gain and $V_{CE(sat)}$ would have to be loosened, and the overall circuit efficiency might suffer slightly.

Finally, a better technique for clamping the duty cycle of the one-shot, N1 (see Figure 7), could possibly reduce the magnitude of the transients which occur during initial turn-on of the inverter. A different clamping approach is being investigated for use in the 100-VA direct-coupled inverter.

SECTION III
SPECIAL COMPONENTS

A. TXCO

The X-1617706-1, 2.4576-MHz temperature-compensated crystal oscillator (TXCO) was obtained as a complete subassembly from the Pioneer-Central Division of Bendix Corporation on a contract basis. The TXCO is packaged in 1 cubic inch. It achieves good frequency stability over a wide temperature range without use of an oven by employing the proper combination of a crystal, a variety of semiconductors, and temperature-compensating passive elements.

The frequency stability versus temperature was ±15 PPM from -25°C to +110°C and ±25 PPM from +110°C to +125°C. Frequency stability data furnished by Bendix and a case outline drawing of the oscillator are given in Appendix D.

B. ISOLATED COMMON TERMINAL

Problems arose during the breadboard development because of the grounding techniques used. During open-loop tests, operation of one part of the system would cause a malfunction of another part. At this time a bus bar was used as a common terminal for connecting the -28-V input to the negative terminals of all the subscripts. It was determined that the malfunction problem was a function of location of the subcircuit "negative return" wires on the bus bar. The conclusion was that the interaction of subcircuits was due to the many "negative return" currents traversing the same length of bus bar.

In order to have a common terminal with equal but separate paths to the —28 V potential a circular common terminal was conceived. It was a cylindrical piece of conducting metal (see Figure 26) with a hole drilled in the center for the —28 V input wires, as well as holes along the outside edge of the top surface for attaching "negative return" wires of subcircuits. Amount of improvement in circuit performance due to using the common terminal was hard to determine accurately, but it was judged to be significant enough to cause adoption of the approach.

It was deemed best to mount the cylindrical common terminal on a stud. Isolation of the stud and cylindrical top was necessary, however, since the case (which is grounded) and the —28 V input are not common. Consequently the isolated common terminal was designed to combine a threaded hexagon-headed stud with a terminal disc, maintaining electrical isolation by means of an aluminum-oxide disc. The initial design consisted of an alloyed sandwich structure of a copper disc, tungsten disc, alumina disc, tungsten disc, and a threaded copper stud. The terminal copper disc was provided with 24 holes around the periphery and a center buss hole for connecting the —28 V terminal. The tungsten was incorporated into the structure to accommodate the expansivity mismatch between copper and alumina.

Due to mechanical problems in this design a different system using a sandwich of invar, alumina, and invar stud was adopted. This system was structurally superior

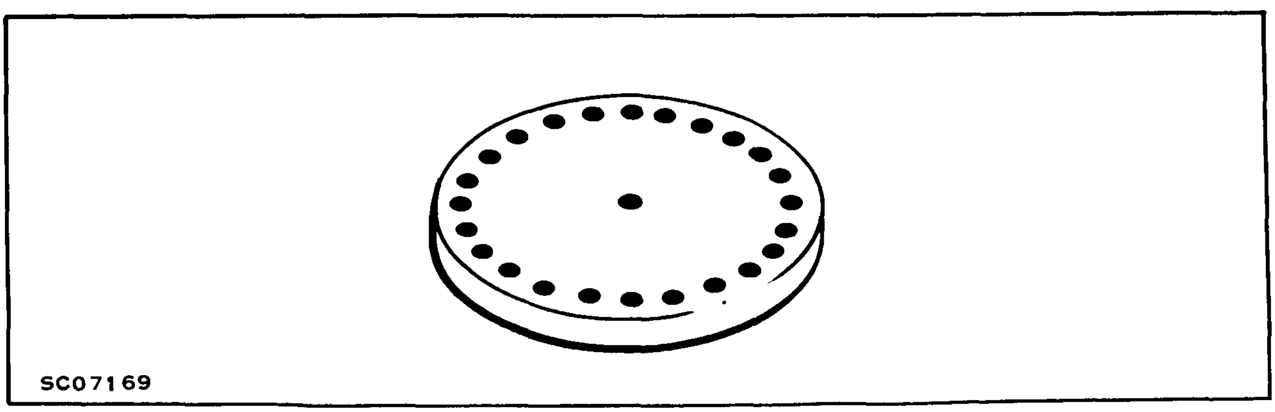


Figure 26. Common Terminal

due to the very low expansivity of invar. It also resulted in lower weight and the use of reduced numbers of piece parts. Structure of the isolated common terminal is shown in this report's Supplement, Exhibit A.

C. VARIABLE-DUTY-CYCLE ONE-SHOT (L-169)

The integrated-circuit, variable-duty-cycle one-shot and the discrete components directly associated with its operation are shown in Figure 27. Purpose of this circuitry is to convert the varying dc voltage to a varying-duty-cycle pulse train.

With this circuit the position of the trailing edge M of the output pulse train (Figure 28) is determined by the dc error voltage. The trailing edge can be moved from M to L for a maximum duty cycle (i.e., the L-164 is ON most of the time) or to N for a minimum duty cycle.

The L-169 is a mask modification of the SN5380 integrated-circuit one-shot. Pins 1, 2, 14, 12, 13 are unused in this circuit configuration. The internal diodes connected between pins 1, 2, and 3 represent an unsuccessful attempt to integrate diodes D2 and D3. Junctions better left reverse biased become forward biased when these integrated diodes are used.

To understand operation of the circuit, consider the condition where there is no voltage on Pin 6. Hence Q1 is OFF; Q2 is ON; Q3 and Q4 are OFF; Q7 is ON because of base drive through R23; Q6 is OFF, and Q5 is ON. In this case C14 will charge up to V_{CC}–Vx through Q5, D3, and D10, and the output (pin 10) is a low voltage. D2 will be reverse biased. With application of a positive going voltage on pin 6, Q1 goes ON, Q2 goes OFF, and Q3 goes ON; consequently pin 9 of the L-169 is almost at ground potential, while the other side of C14 is at a negative voltage of $|V_{CC} - Vx|$. D2 is forward biased by this voltage and the base emitter of Q7 is reverse biased, and consequently Q7 if OFF and the output is high.

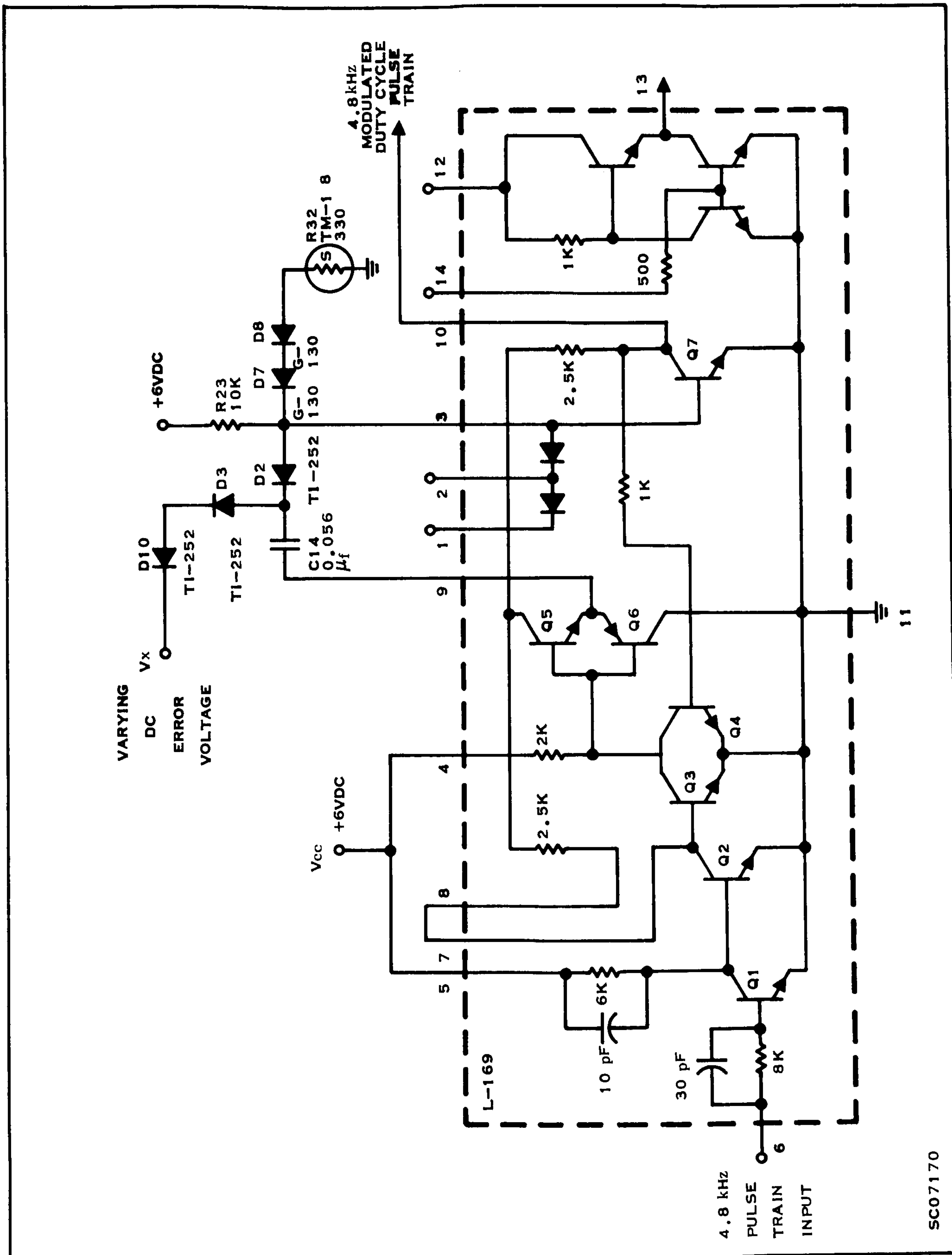


Figure 27. Variable Duty Cycle One-shot and Associated Circuitry

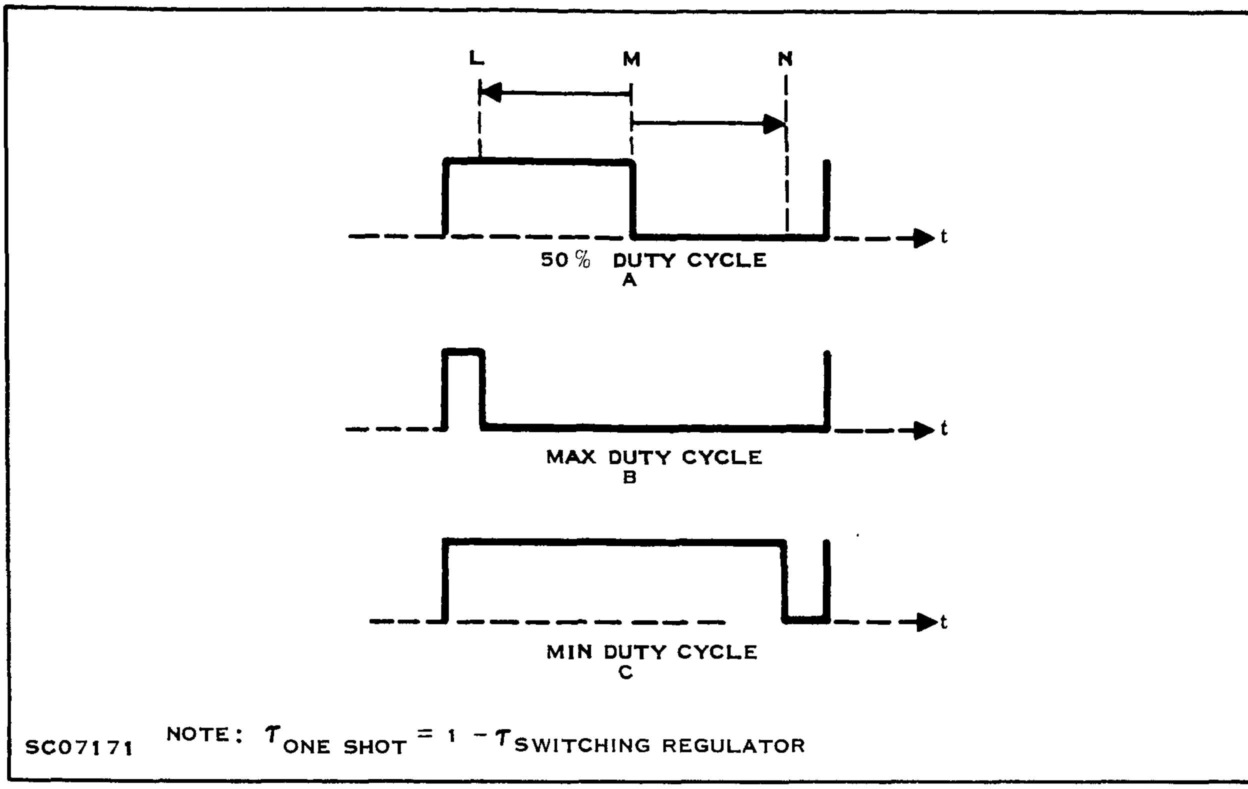


Figure 28. Variable Duty Cycle One-shot Output Waveforms

The output stays high for as long as the voltage on C14 is negative enough to reverse-bias the base-emitter junction of Q7. C14 will lose its negative potential by being charged positively through R23, D2, and Q6. Length of time the output remains high is then primarily a function of the values of R23, C14, Vx, and V_{CC}. All are held relatively constant except for Vx, resulting in the duty cycle of the output being a function of Vx.

A plot of the transfer characteristic of this circuit is shown in Figure 29. The circuit is capable of operation to 100 percent duty cycle but not 0 percent duty cycle. As 0 percent duty cycle is approached there is sufficient time for C14 to charge up to the appropriate negative voltage. This will result in the output operating at one-half of the proper frequency. To keep this from happening a clamp is used to prevent the circuit from reaching a low value of duty cycle. In Figure 27 the clamp function is performed by D7, D8, and R32. Details of electrical evaluation are presented in Appendix E.

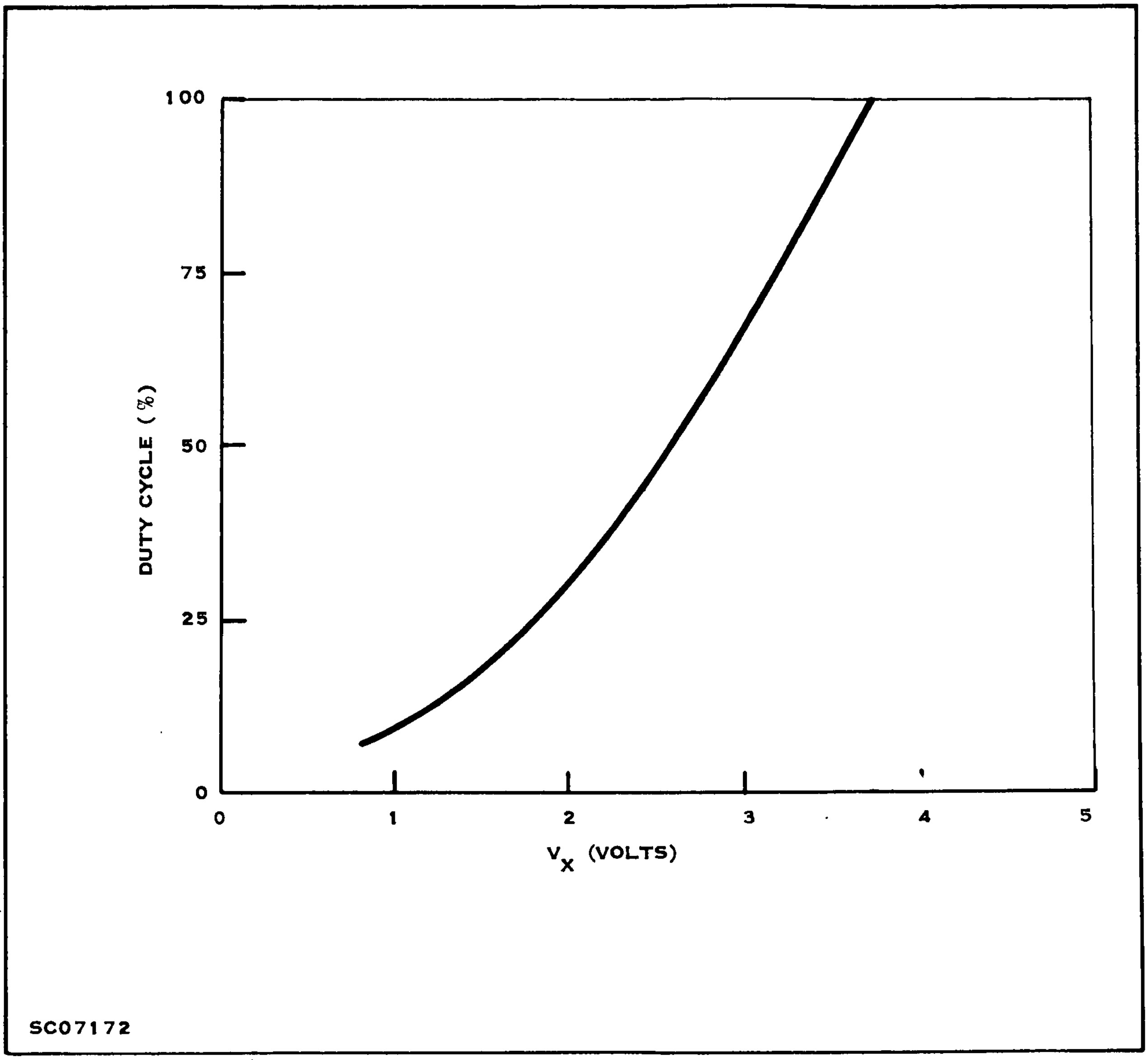


Figure 29. Voltage Transfer Characteristic

SECTION IV

POWER-DEVICE DEVELOPMENT

A. DESCRIPTION OF DEVICE REQUIREMENTS

1. Electrical Requirements

Prime requirement of the L-163 is that it switch a moderately high current while being driven by the output of a low-current integrated circuit. This means that the device must switch a load current of 2.0-2.5 amps with a gain of 1000 at a temperature of -25°C. The on-voltage of the switch should also be low to maximize circuit efficiency. In the off state the switch must exhibit a sustaining voltage of at least 65-80 volts.

The L-163 switches operate at a low power level, but the L-163 in the power supply for low-level circuitry functions in a linear mode and must dissipate approximately six watts. The L-163 must also be free from second breakdown for the energy levels it experiences in the circuit.

The L-164 must operate as a high-gain, high-current PNP transistor. This operation can be achieved by driving an NPN transistor with a PNP as seen in Figure 30. The composite device must carry a load current of 10 A with a gain of 500-2,000 at -25°C, and have a sustaining voltage greater than 60 V.

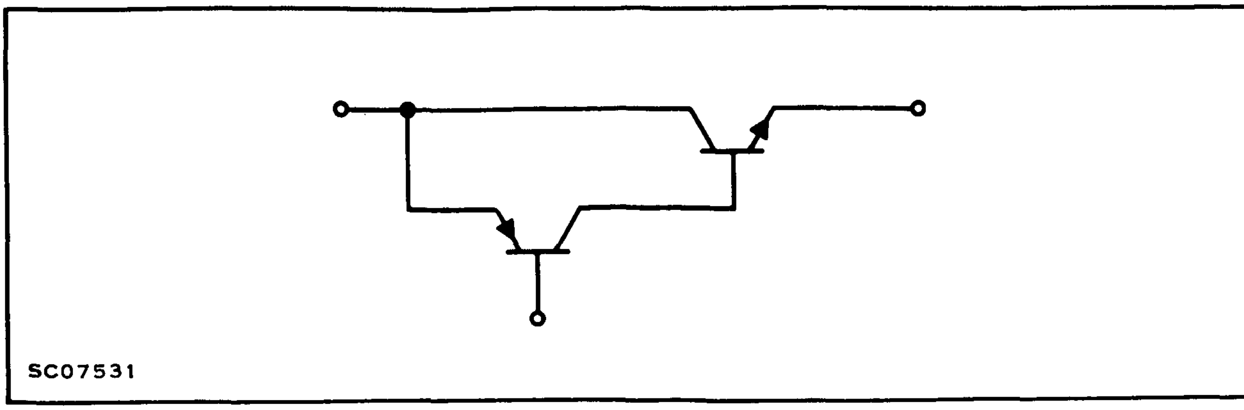


Figure 30. L-164 Complementary Arrangement

2. Package Requirements

The preferred design for integrating two power devices was found to be a six-lead electrically isolated hexagon-stud package. The package consists of an age-hardenable copper-alloy threaded stud (for superior mechanical properties) to which an OFHC copper cold-weld flange is attached for reliable sealing using TI "split-die" cold-weld technique. The wafers are mounted on metallized BeO pads, which provide electrical isolation and good thermal-conductivity properties. Six silver pins, serving as stud terminals, are electrically isolated from the stud by aluminum-oxide discs. The mating cap consists of six hermetically sealed flattened and pierced copper tubes attached to a ceramic pin spacer having an annular OFHC copper cold-weld flange.

The L-163 and L-164 packages are similar except for the BeO substrates, which are designed to accommodate different-size silicon wafers. L-163 and L-164 packages are shown in the Supplement, Exhibit B.

B. HISTORY OF DEVELOPMENT

1. L-163 Wafer Development

a. Determination of Wafer Geometry and Process

The high-gain requirement for this device indicates the necessity for a darlington configuration giving a gain which is the product of the gains of two transistors. Figure 31 shows the 2N3837 wafer produced by the Power department of Texas Instruments. The data sheet shows the following specifications for this device type:

$$V_{(BR)CEO} \geq 80 \text{ V at } I_c = 30 \text{ mA}$$

$$h_{FE} = 2,000 - 20,000 \text{ at } V_{CE} = 2 \text{ V}, \ I_C = 2 \text{ amp}, \ T = 25°C$$

These specifications indicate that the 2N3837 wafer should be satisfactory for the L-163.

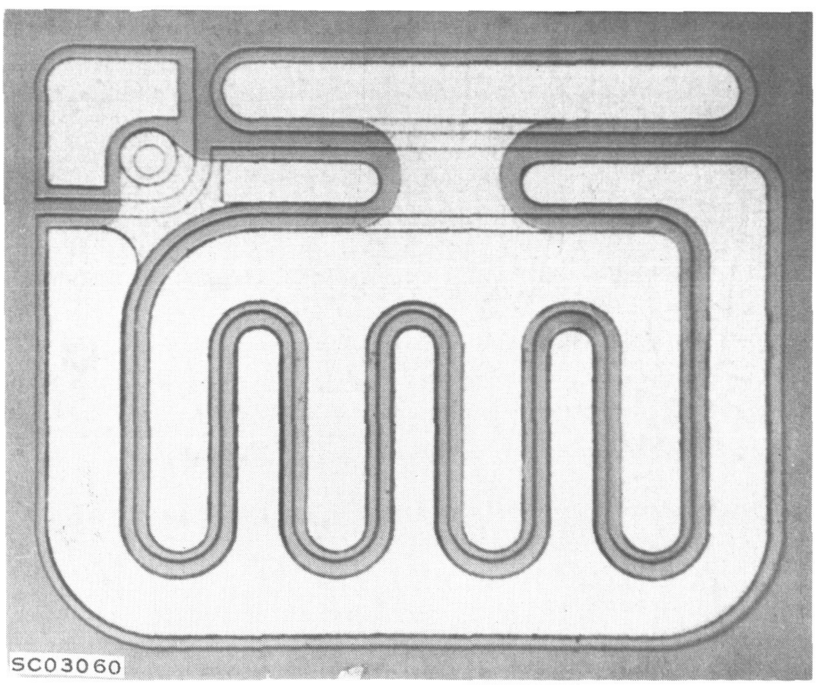


Figure 31. 2N3837 Wafer

Several devices were built in single packages for evaluation of this wafer and experimental use in the system. These devices satisfactorily withstood energies of 440 millijoules in the second breakdown test. (An explanation of this test is given later.) The data on these devices and their satisfactory circuit operation indicated that this wafer was quite satisfactory.

Four different approaches were investigated, all utilizing the basic 2N3837 geometry. The A approach consists of mounting two separate chips in the same package. Since this approach was chosen to build the required devices, a complete description of the process will be deferred until later in this report.

The other three approaches offered a higher level of integration, as two electrically isolated darlingtons were combined in a single chip of silicon. This integration necessitates a collector contact on the water's top surface which is not present on the standard 2N3837 wafer. Masks were modified to provide this contact area; Figure 32 shows the revised contact pattern. This geometry was used for the B, C, and D integrated approaches, described below.

b. Integration Approaches and Results

(1). Integration Approach B

As outlined in Figure 33, this process begins by oxidizing one side of a low-resistivity N-type silicon slice. Polycrystalline silicon is next epitaxially deposited over the oxide and the original material is lapped to a thickness of 4.0 ± 0.5 mils. An epitaxial layer of 5 Ω-cm N-type silicon is then grown on the original material.

The standard planar epitaxial transistor structure can now be formed by diffusing a base and emitter into the 5 Ω-cm epitaxial layer. The polycrystalline silicon provides a mechanical backing electrically insulated from the

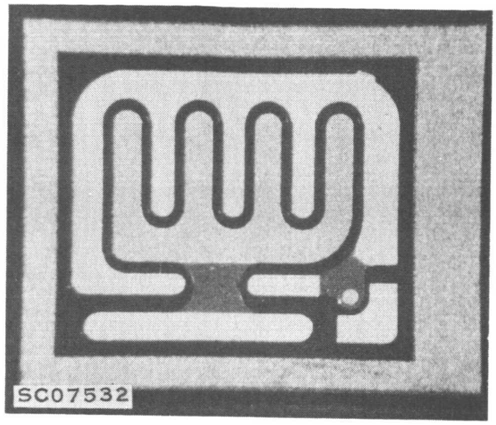


Figure 32. Revised Contact Pattern for 2N3837 Wafer

active portion of the structure. An N^+ diffusion is necessary under the top collector contact to provide low-contact resistance. Electrical isolation between transistors is provided by etching a moat through the single crystal silicon.

(2). Integration Approach C

This integration approach is outlined pictorially in Figure 34. Again starting with a low-resistivity N-type slice, a grid pattern of isolation grooves is etched on one side. Next an oxide is grown on the grooved side of the slice, followed by an epitaxial deposition of thick polycrystalline silicon. The original material is then lapped until the grooves isolate the islands of original material. An area in the center of each island is next etched out and filled with epitaxial 5 Ω-cm N-type silicon. The transistor can now be formed by diffusion in this area. The low resistivity of the original material makes it unnecessary to do an H^+ diffusion for the collector contact.

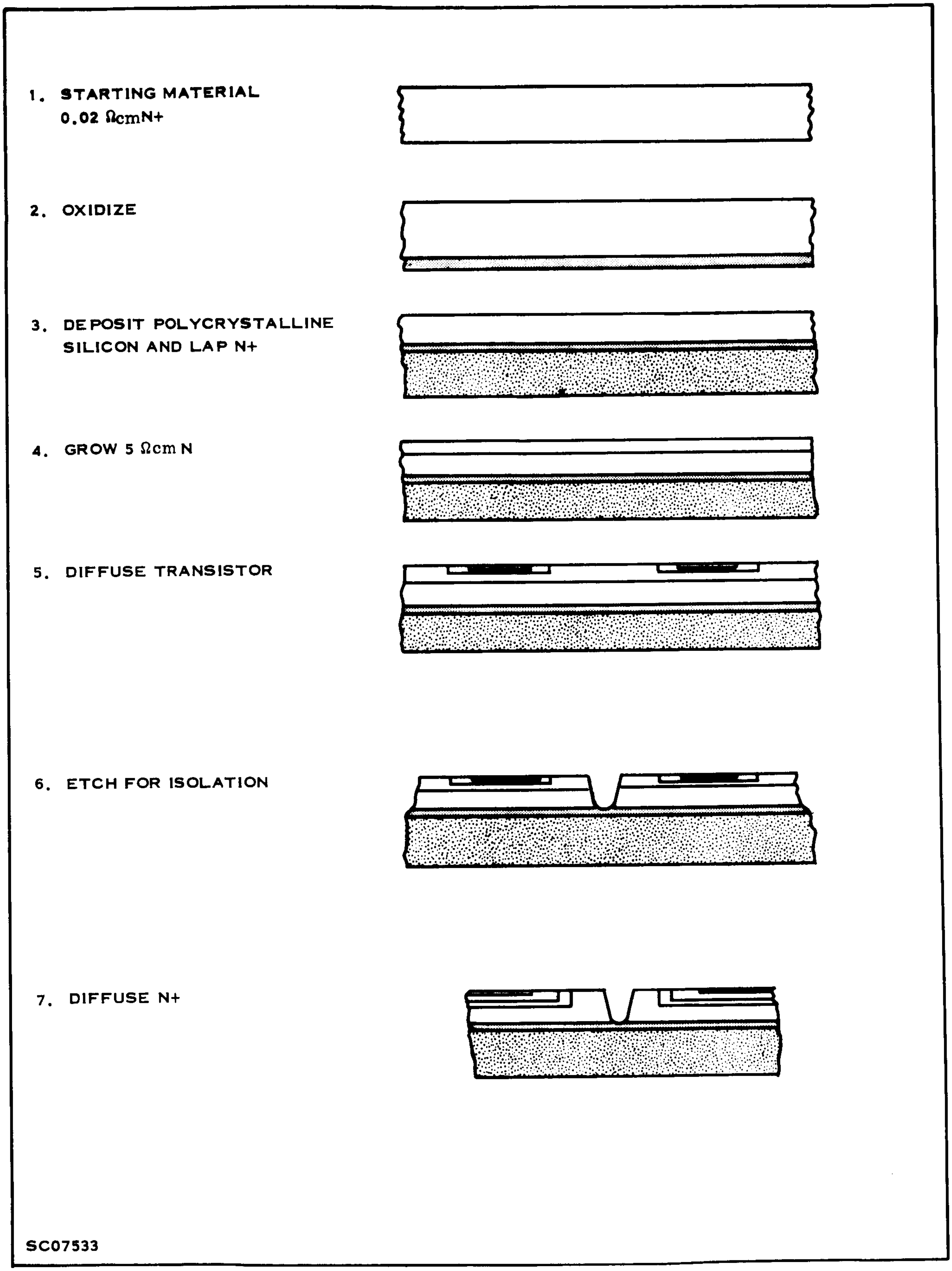


Figure 33. NASA Inverter Power Transistor, Approach B

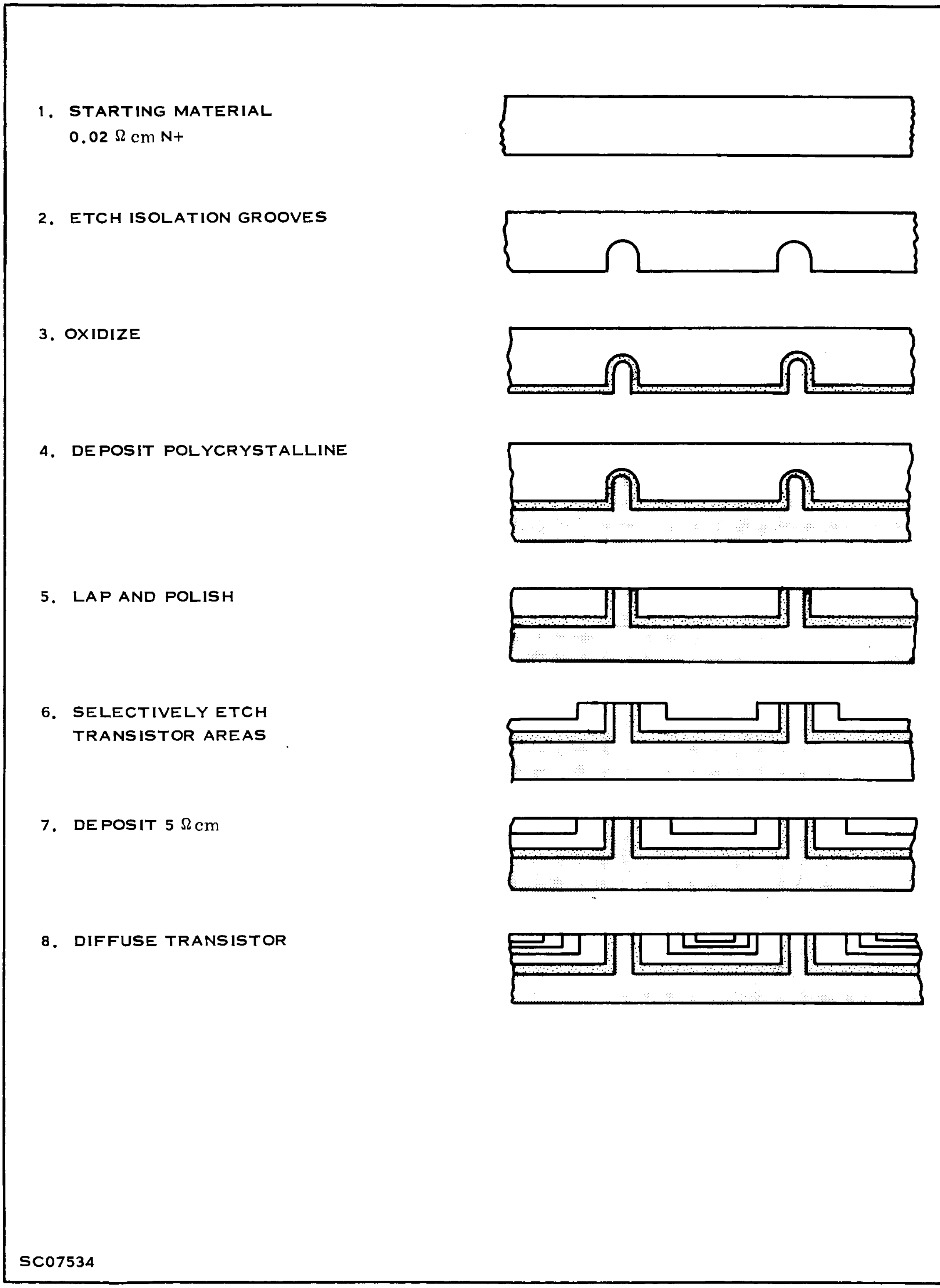


Figure 34. NASA Inverter Power Transistor, Approach C

(3). Integration Approach D

Method of isolation for this approach is the same as for the C process. Figure 35 outlines the D process, which starts with 5 Ω-cm silicon and does not require the "selective etch and refill" epitaxial technology. An N^+ diffusion into the grooved side prior to oxidation provides a low-resistance top collector contact. Oxide growth, polycrystalline deposition, and lapping proceed as for the C process. The transistor is then formed by diffusion into the islands of original material.

(4). Results of Integration Attempts

Aside from the additional difficulties caused by the integration schemes themselves, all three approaches have a common deficiency: the yield to 2N3837 specifications is very low for individual wafers. Therefore the yield of two good adjacent devices is extremely poor. This fact is the prime cause for the decision, early in 1966, to pursue only the dual-chip approach.

Moreover, additional processing required to provide the integration creates further problems. Several runs were unsatisfactory because of difficulties encountered in controlling the lapping process to obtain the desired layer thicknesses. The B approach runs had a high percentage of collector-emitter shorts — apparently a result of the collector contact diffusion, although the cause of failure was never pinpointed. At the time it was attempted the "selective etch and regrowth" technology, basis of the C process, was not well developed.

The D process was the most promising, but its yield of good adjacent devices was very low. The silicon dioxide did not provide reliable isolation; addition of a layer of silicon nitride was necessary for an effective insulating layer. Consequently the recent effort has been devoted only to dual-chip approaches.

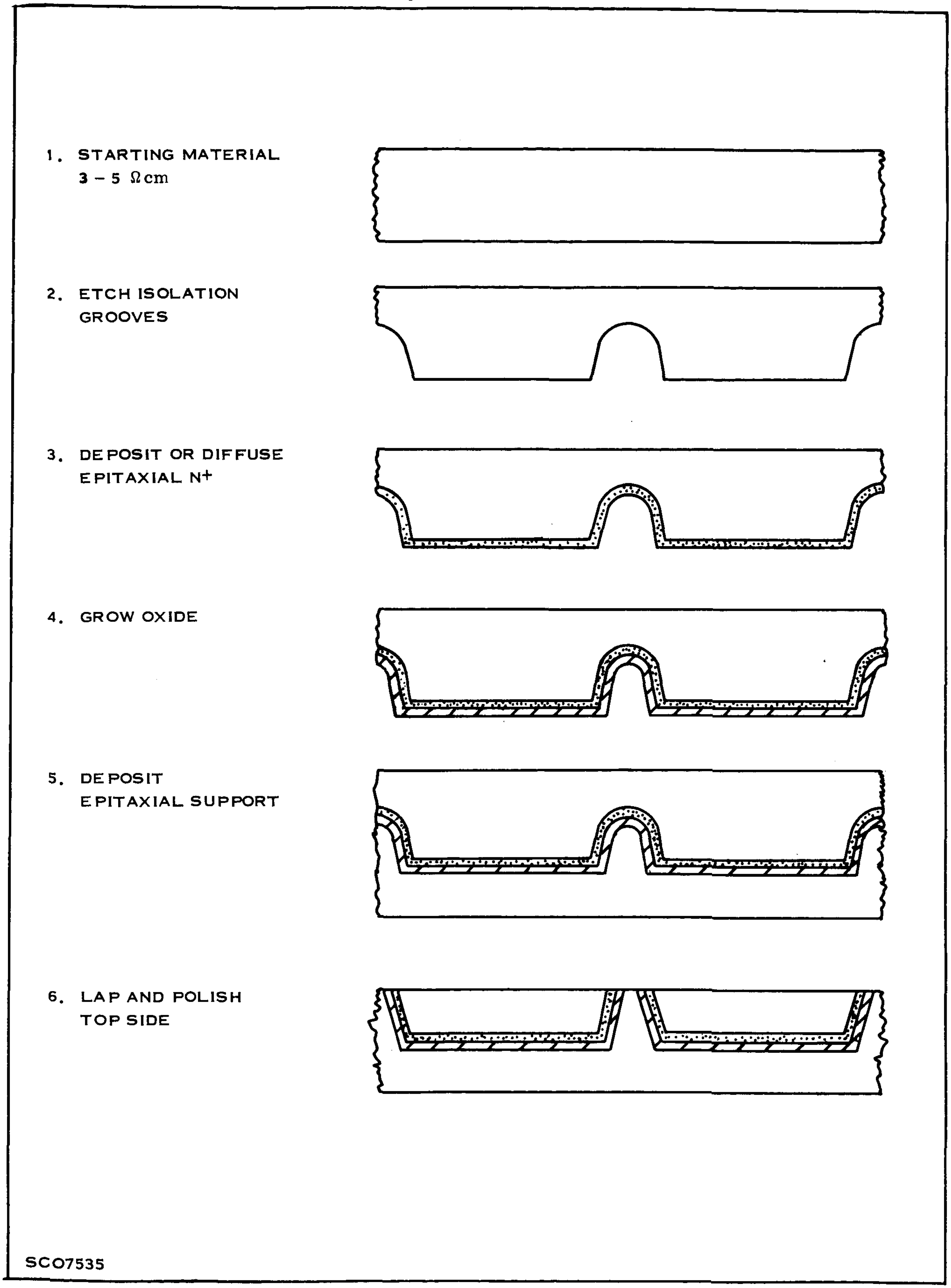


Figure 35. Power Transistor Fabrication Process, Approach D (Sheet 1 of 2)

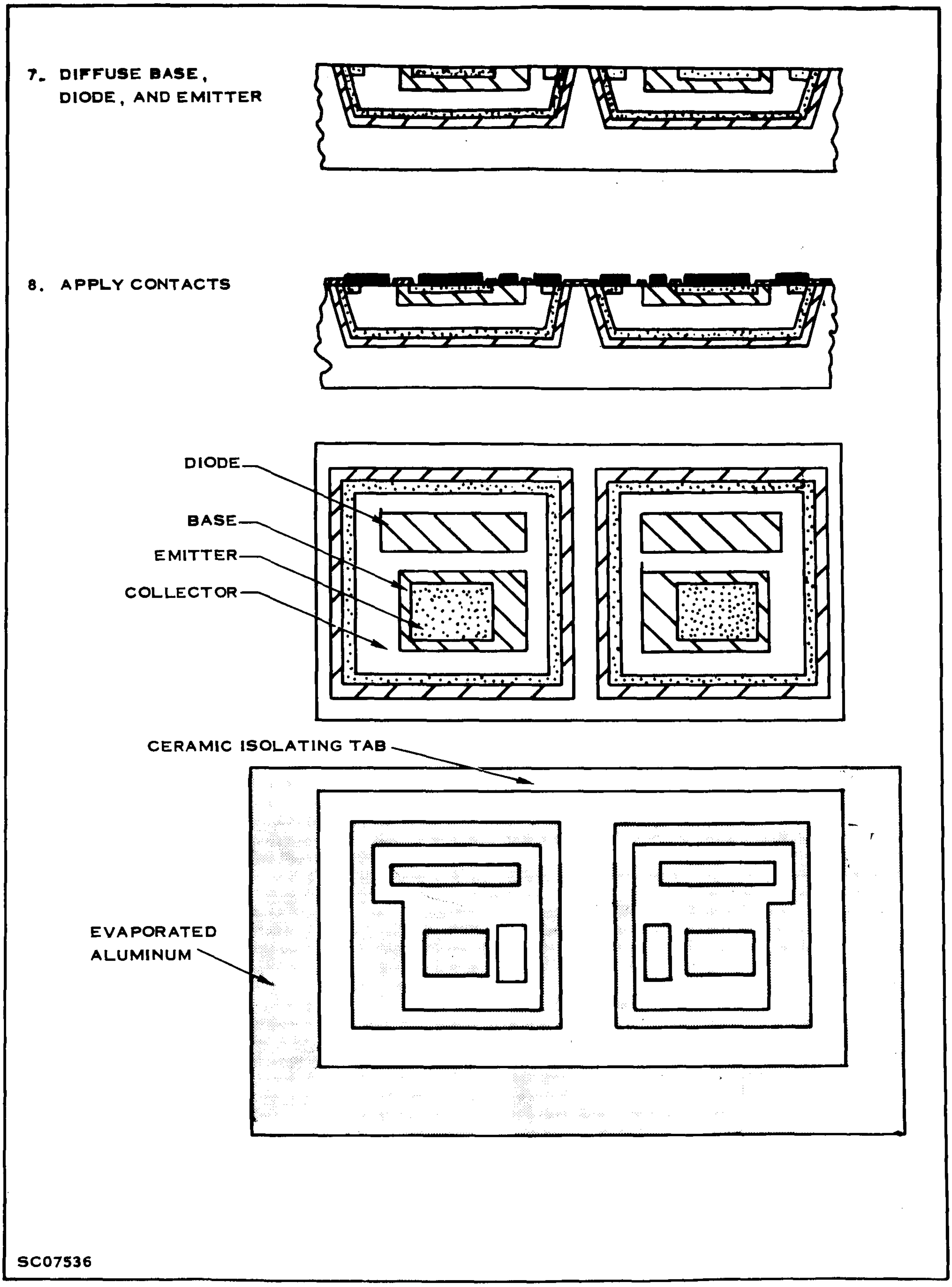


Figure 35. Power Transistor Fabrication Process, Approach D (Sheet 2 of 2)

c. Development of the Dual-chip Approach

The dual-chip approach did not require considerable wafer development, since the process was already available. However, yield under the 2N3837 electrical specifications proved to be a problem. For a given geometry, both $V_{(BR)CEO}$ and h_{FE} are controlled primarily by the base width. It was necessary to lower the $V_{(BR)CEO}$ specification to get units which would satisfy the gain requirement at -25°C. The specification was first lowered to 65 V, but later was raised to 70 V.

The satisfying of these specifications was complicated by two other factors. First, wafers can be probed only at room temperature and at a current level below the 2.5 amps at which h_{FE} is specified. It was necessary to accumulate some data before probe results could be correlated with the first test results. Second, changes of the wafer's surface condition sometimes caused $V_{(BR)CEO}$ to degrade during mounting. These factors all contributed to the low-yield experience for this device.

2. L-164 Wafer Procurement

Basic requirements of this PNP-NPN complementary darlington can be met by using standard wafers from the TI Power department's product line. The XP17 PNP transistor is used for the driver; the 2N4002 NPN transistor for the output device. Initial units fabricated exhibited very high gain, and the circuit was designed to require a current gain of 2000 at 10 amps and -25°C. Subsequent wafers had lower gain, and some difficulty was experienced in satisfying this specification.

C. L-163 PROCESS AND RESULTS

1. Physical Description

The 2N3837 wafer, shown in Figure 31, is produced by the planar epitaxial process. The two transistors and diode are formed by diffusion into a high-resistivity N-type epitaxial layer which has been deposited on a low-resistivity substrate. The epitaxial layer needs only to be thick enough to provide the required breakdown voltage, since the substrate provides mechanical support. For this transistor a 1-mil-thick epitaxial layer of 3-5 Ω-cm phosphorus-doped silicon was used.

2. Packaging Process

Two darlington wafers, mounted in a single package, are isolated from the package stud by means of ceramic pedestals. Six pins serve as electrical terminals which are connected to the transistors by means of aluminum lead wires. The fabricating and packaging process is as follows:

a. Stud Fabrication

Cold-weld flanges are made from OFHC copper rings in a flangeing operation employing a hydraulically operated press. The flange, brazed to an 11/16-inch hexagonal PD-135 copper-alloy stud, uses a ring preform of the silver-copper eutectic brazing alloy.

Six nickel pins, electrically isolated from the copper-alloy stud by metallized alumina discs, and two metallized BeO tabs are simultaneously alloyed to the stud, using vacuum-tube-grade silver-copper eutectic alloy brazing preforms in a reducing-atmosphere furnace operation.

Stud fabrication is completed by brazing two copper collector tabs connecting the ceramic isolation tabs to the collector pins on the package. Drawings in the Supplement, Exhibit B, present details of the piece parts for stud fabrication and assembled stud.

b. Cap Fabrication

Cold-weld flanges, similar to those on the stud, are made from OFHC copper rings. The tools used for this fabrication step are identical with those used during the cold-welding operation except for the punches used in the two cases. Thus exact matching of flanges is achieved during the welding operation.

Six OFHC copper terminal tubes are flattened and pierced at one end and brazed to a circular ceramic pin spacer along with the copper flange. Silver-copper eutectic alloy preform rings are employed for the brazing operation. Terminal tubes are sealed by means of spheres of the same alloy dropped into the tubes before brazing the assembly.

Details of piece parts and assembled cap are shown in the Supplement, Exhibit B.

All brazing operations are carried out by assembling piece parts in graphite boats and heating to the required temperature in chain furnaces which employ a reducing atmosphere.

Flange surfaces on the stud and cap are electroplated with an alloy of nickel-tungsten using a brush plating process. This operation, providing an optimum surface property for the most effective cold weld, is superior to barrel or electroless plating techniques, either of which would require careful masking of all internal stud components.

c. Contacts

Evaporated aluminum top contacts and electroless nickel collector contacts are used on these devices. The collector surface of the slice is activated and plated with electroless nickel and the nickel sintered at 630°C in dry nitrogen.

This nickel is leached to remove nickel and nickel oxides, and the slice is transferred to the evaporator for top contact deposition. One mg of aluminum is evaporated at a distance of 3-1/2 inches from the slice, which is placed on a quartz plate. The aluminum is microalloyed and an additional 700 mg of aluminum evaporated onto the slice from a distance of 4 inches.

Following a KMER and aluminum leach operation a second layer of electroless nickel is applied on the nickel silicides remaining on the collector surface. Following metallization the slice is scribed and broken into individual wafers.

d. Wafer Mounting and Final Assembly

The wafers are mounted on the metallized BeO isolation tabs in the package by furnace alloying, using gold-germanium preforms and a nitrogen atmosphere. Aluminum wires are ultrasonically welded to the emitter and base regions of the wafers. The other ends of these wires are resistance welded to the designated terminal pins.

The package is sealed by cold welding, employing a split-die cold-weld apparatus. Cold-weld joining leads to stress-free, weld-flash-free hermetic sealing.

Packaging is completed by gold-plating the devices for corrosion resistance and ease of soldering; 125 micro-inches of gold is plated on a nickel substrate.

3. Electrical Evaluation and Results

a. Electrical Specifications

Table I lists a portion of the electrical specifications to which the L-163's were 100 percent tested. In addition the devices underwent a test for second breakdown and an operating test. To pass the second-breakdown test, transistors were required to turn off a current of 10 amps flowing through an 880-μH inductor. Energy stored in the inductor is dissipated by the transistor conducting the decaying current at its collector-emitter breakdown voltage.

The six-watt operating test utilizes the circuit shown in Figure 36. This test was performed for 20 hours in a 125°C ambient. The transistors conduct 0.6 A collector current with $V_{CE} = 10$ V. The devices which fail draw excessive collector current because of the generation of free carriers by heat. Some early units were evaluated to a thermal impedance test in place of the operating test.

Table I. L-163 Specifications

	Test Parameter (T_C = 25°C Unless Noted)	Min.	Max.	Unit
$V_{(BR)CEO}$	$I_C = 30$ mA, $I_B = 0$	70.0		V
I_{CEO}	$V_{CE} = 50$ V, $I_B = 0$		100.0	μA
$V_{CE(sat)}$	$I_B = 2.5$ mA, $I_C = 2.5$ A	0.7	1.1	V
	$I_B = 2.5$ mA, $I_C = 2.5$ A $T_C = -25$°C		1.4	V
$V_{BE(sat)}$	$I_B = 2.5$ mA, $I_C = 2.5$ A	1.4	1.9	V
	$I_B = 2.5$ mA, $I_C = 2.5$ A $T_C = -25$°C		2.0	V
V_{CEF}	$I_C = -2.5$ A, $I_B = 0$		1.3	V
I_{CES}	$V_{CE} = 50$ V, $V_{BE} = 0$ $T_C = 150$°C		10.0	mA

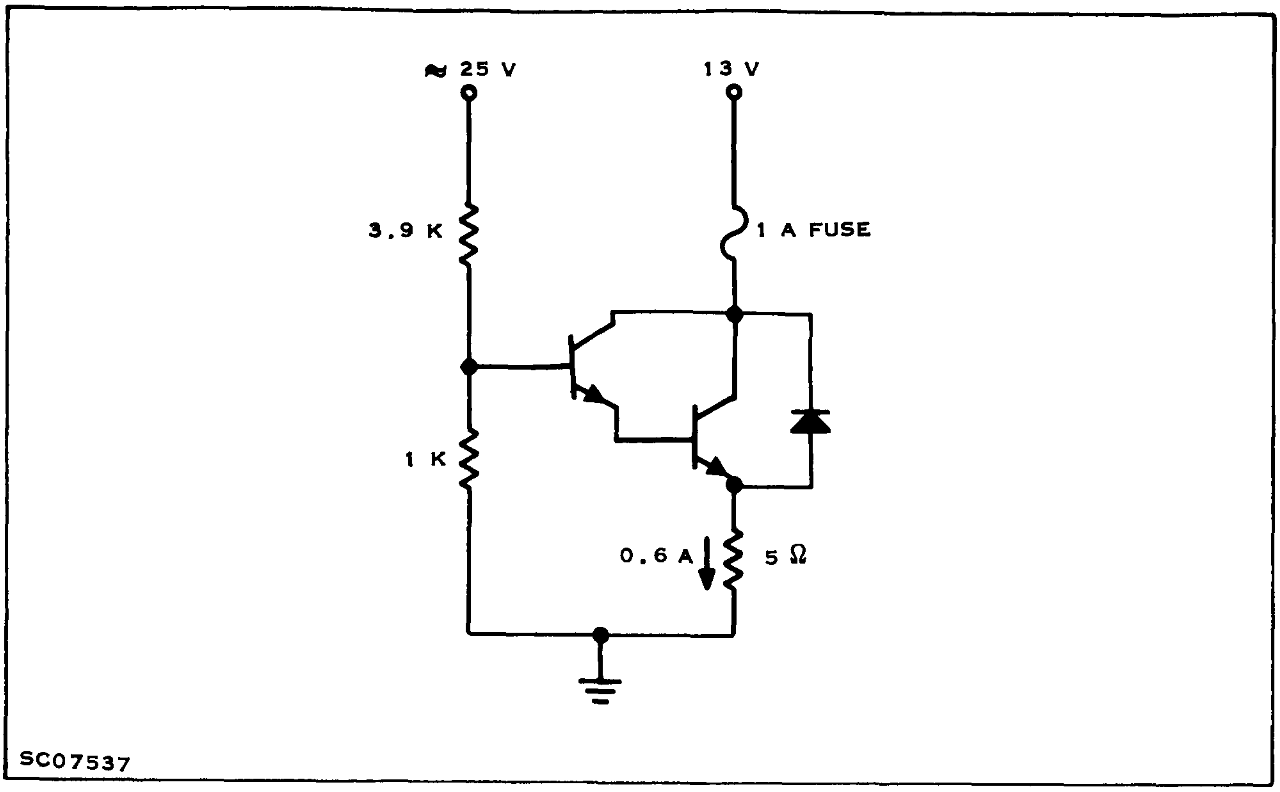


Figure 36. Operating Test Circuit

b. Results

Figure 37 displays the trade-off between $V_{(BR)CEO}$ and current gain. The percent of units in each voltage range which fail to meet the -25°C $V_{CE(sat)}$ specification is displayed in the figure. This $V_{CE(sat)}$ specification is shown since it reflects the losses incurred because of low gain. It can be seen that for $V_{(BR)CEO} >$ 75 V the gain specification becomes increasingly difficult to meet for higher $V_{(BR)CEO}$.

Of all units tested only 11 percent were rejected because of failure to pass the 10-amp second-breakdown test. A single run of devices, which would not satisfy other specifications, accounted for over half of this 11-percent loss. The devices proved to be capable of operation at high energy levels.

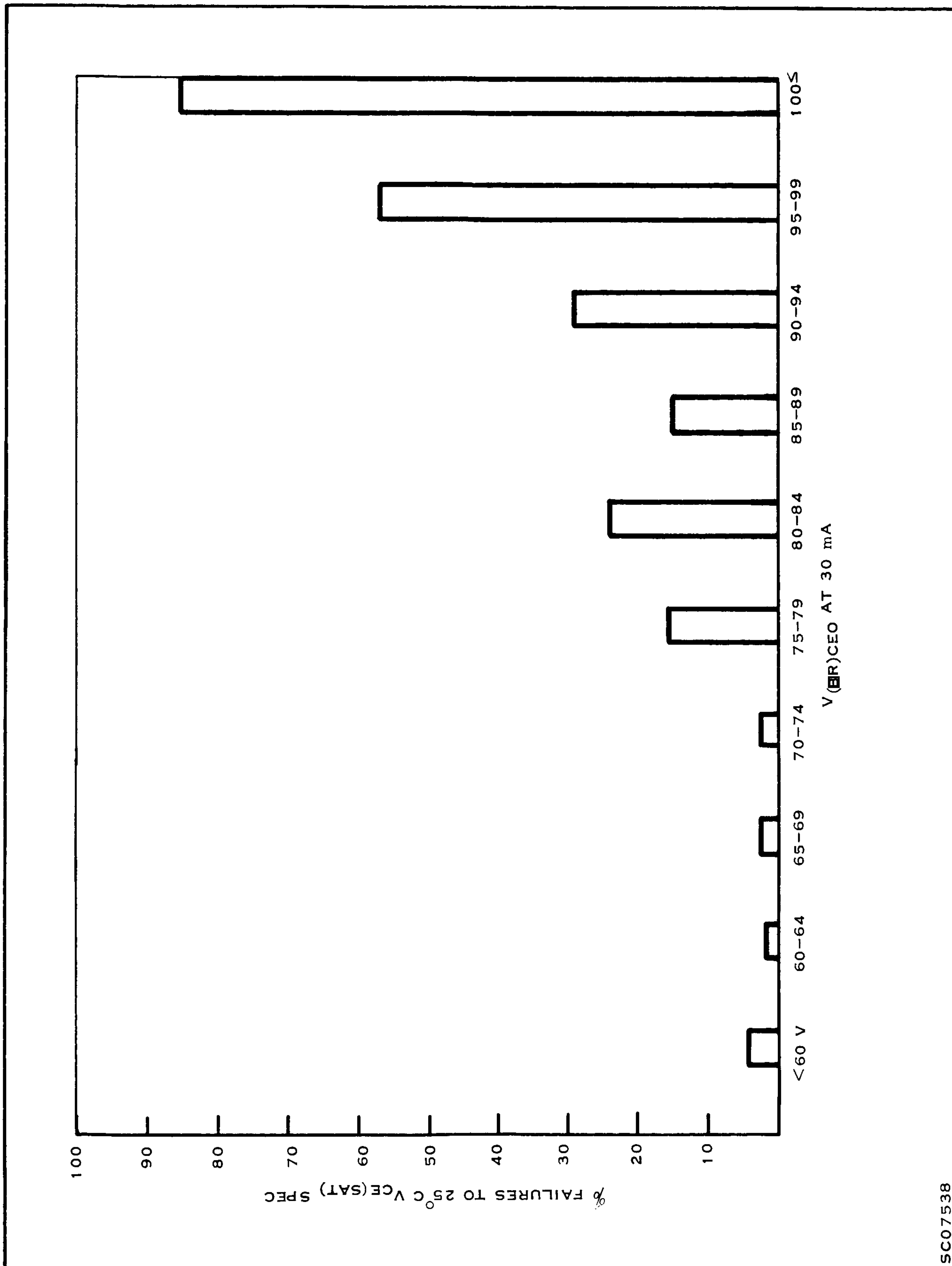


Figure 37. Effect of $V_{(BR)CEO}$ Distribution Upon -25°C Gain

D. L-164 PROCESS AND RESULTS

1. Physical Description of Wafers

Both of the wafers used for this device are fabricated by standard planar epitaxial techniques. The PNP driver is a 90 x 90-mil silicon chip while the NPN output transistor is a 200 x 200-mil chip. These wafers mounted in the stud assembly are seen in the Supplement, Exhibit B.

2. Packaging Process

This package contains an NPN and a PNP transistor mounted on two isolated BeO tabs. The package is similar to the L-163 package except for having different-sized isolation ceramics to accommodate the two wafers of differing sizes. The copper collector tabs used in the L-163 package are eliminated in this package, and collector pin terminals are directly brazed to the ceramic isolation tabs. (See drawing SRDL-ISI-85 in the Supplement, Exhibit B.)

The contacts on the NPN wafer consist of electroless nickel collector contacts and evaporated aluminum top contacts. The PNP wafer which is of smaller geometry has aluminum top contacts and no collector contacts.

The PNP wafer is scrub mounted to the BeO isolation ceramic, using a gold-silicon preform. The ceramic pedestal is gold plated prior to the alloying operation for better wettability. The NPN wafer is then furnace alloyed on the larger ceramic base, using a gold-germanium preform. Aluminum wires are sonobonded to transistors and welded to the terminal pins. A drawing of the completed assembly is shown in the Supplement, Exhibit B.

The package is closed by cold-welding the cap to the stud and gold-plating the completed unit, as in the L-163 assembly described above.

3. Evaluation and Results

Basic requirements of this device are shown in Table II. In addition to these specifications, the device was tested for second breakdown. To pass the test the device is required to sustain 20 V and 20 A for 10 ms.

Since the gain of this composite device is the product of the transistors' individual gains, variation in the individual transistor gains causes considerable variation in the composite gain. Probe data do not allow accurate prediction of the high-current gain of the NPN, as the probes will not carry high current. For this reason some yield loss was experienced because the composite gain was too low.

Table II. L-164 Specifications

	Test Parameter (T_C = 25°C Unless Noted)	Min.	Max.	Unit
$V_{(BR)CEO}$	$I_C = -30$ mA, $I_B = 0$	60		V
h_{FE}	$I_C = -10$ A, V_{CE} -2.5, $T_C = +25°C$	4500	1200	
$V_{CE(sat)}$	$I_B = -5$ mA, $I_C = -10$ A, $T_C = -25°C$		1.5	V
θ_{J-C} - NPN			4.0	°C/W
I_{CES}	$T_C = 150°C$, $V_{CE} = -50$ V		10	mA

E. RECOMMENDATIONS

Primary causes of the low yields experienced with these power devices are:

1) The wafer cannot be produced to meet all specifications with a high yield.

2) Requirements of a dual-chip, isolated package make the assembly process long and complicated.

Size of the wafer, and the added complexity of the darlington configuration, indicate that a very high yield should not be anticipated. Since item 2 amplifies the difficulties of item 1, the advantages of packaging two devices together should be re-evaluated.

SECTION V
INTEGRATED-CIRCUIT ARRAYS

This development program required four array types for the inverter system: a ÷ 10 counter, a ÷ 12 counter, a ÷ 256 counter, and a six-stage Johnson (folded-ring) Counter with clocking driver. These four arrays comprise the timing section of the power inverter. A "master slice" is used for the ÷ 10, ÷ 12, and ÷ 256 counters; i.e., a common set of diffusion masks is used for all of these counters, but the metallization pattern is different for these arrays.

Development and production were successful for the ÷ 10, ÷ 12, and ÷ 256 arrays but not for the Johnson Counter array (L-165). After an initial run which produced a number of arrays operating almost within specifications, the yield dropped to zero and, despite concentrated effort, remained there. Consequently, in the production inverters, standard series 53 integrated circuits and discrete resistors were used to perform the Johnson Counter function. Johnson Counter performance and specifications covered in this section are applicable only to the L-165.

A. DISCUSSION

Operating requirements for the integrated-circuit arrays developed for this program did not include the use of very-high-speed circuits. Nevertheless, physical constraints imposed by the degree of complexity of the monolithic arrays dictated the use of small-device geometries to minimize the amount of surface area required for a given array. By using small geometries for the transistors, in particular, high-frequency operation becomes an inherent characteristic of the array. The geometries of circuit devices used in this program are quite similar to those used in the Series 54/74 catalog line being produced by Texas Instruments. As a result, arrays were produced with capability of operation with clock frequencies in excess of 10 MHz.

Electrical specifications for these integrated-circuit arrays are as follows:

L-166 Ripple Counter ($\div 2^8$)

Frequency input to counter: . .	2.4576 MHz
Frequency output of counter: .	a) 19.2 kHz
	b) 9.6 kHz
Input levels:	a) true state +1.9 V_{min}
	b) false state +0.35 V_{max}
Output levels:	a) true state +2.5 V_{min}
	b) false state +0.3 V_{max}
Power supply:	4.5 V ± 0.5 V
	I_{max} = 94 mA

L-168 Decade Counter ($\div 10$)

Frequency input to counter: . .	19.2 kHz
Frequency output of counter: .	1.92 kHz
Input levels:	a) true state +1.9 V_{min}
	b) false state +0.35 V_{max}
Output levels:	a) true state +2.5 V_{min}
	b) false state +0.3 V_{max}
Power supply:	4.5 V ± 0.5 V
	I_{max} = 51 mA

L-167 ÷ 12 Counter

Frequency input to counter: . .	19.2 kHz
Frequency output from counter: .	1.6 kHz
Input levels:	a) true state +1.9 V_{min}
	b) false state +0.35 V_{max}
Output levels:	a) true state +2.5 V_{min}
	b) false state +0.3 V_{max}
Power supply:	+4.5 V ± 0.5 V
	I_{max} = 51 mA

L-165 Johnson Counter

Frequency input to counter: . .	9.6 kHz
Frequency output from counter: .	a) 4.8 kHz
	b) 400 Hz (12 outputs at 30° increments)
Input levels:	a) true state +1.9 V_{min}
	b) false state +0.35 V_{max}
Output levels:	1) 4.8 kHz
	a) true state +3.0 V_{min}
	b) false state +0.3 V_{mix}
	2) 400 Hz
	a) true state +2.5 V_{min} at 2.5 mA
	b) false state +0.3 V_{max}
Power supply:	+5.7 V ± 0.5 V
	I_{max} = 91 mA

Schematics and block diagrams of the arrays are shown in the accompanying figures: Figure 38, Ripple Counter Flip-flop; Figure 39, Array Interconnection; Figure 40, Johnson Counter Block Diagram; Figure 41, Johnson Counter Flip-flop.

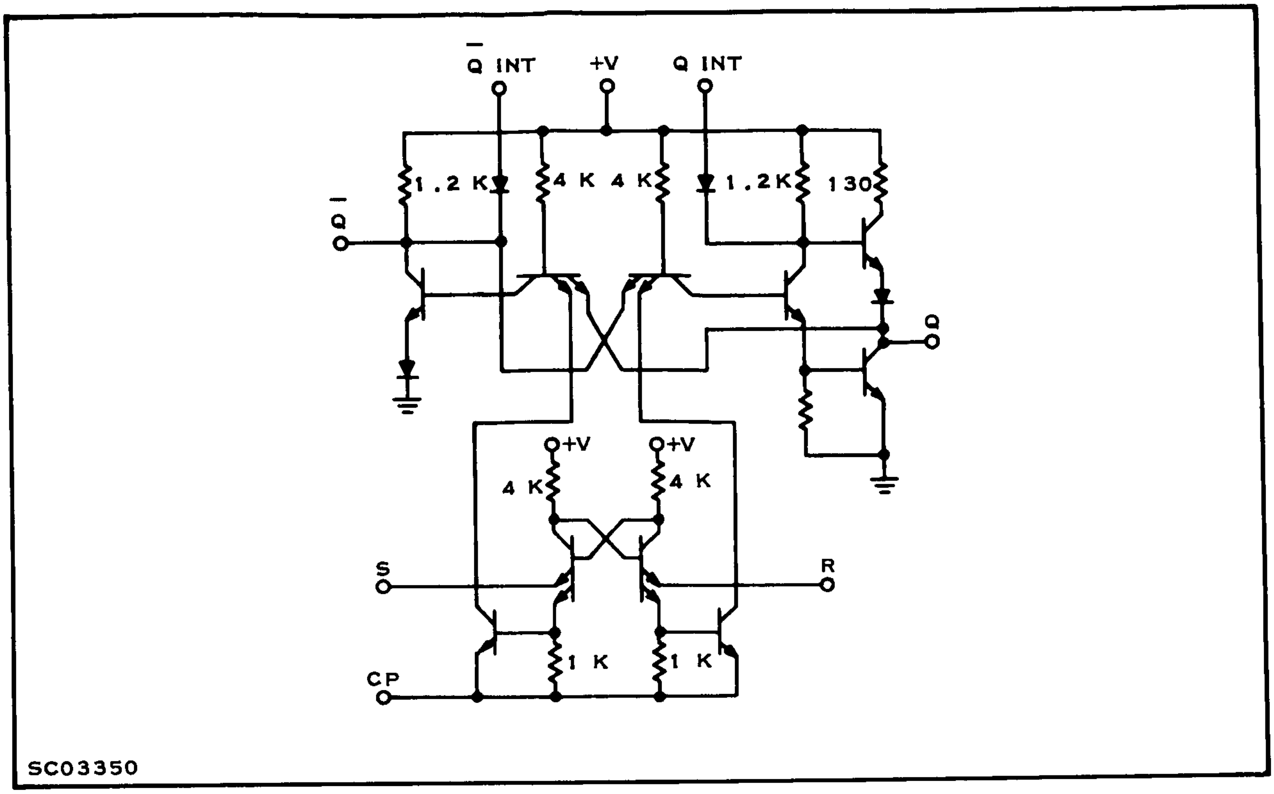


Figure 38. Ripple Counter Flip-flop

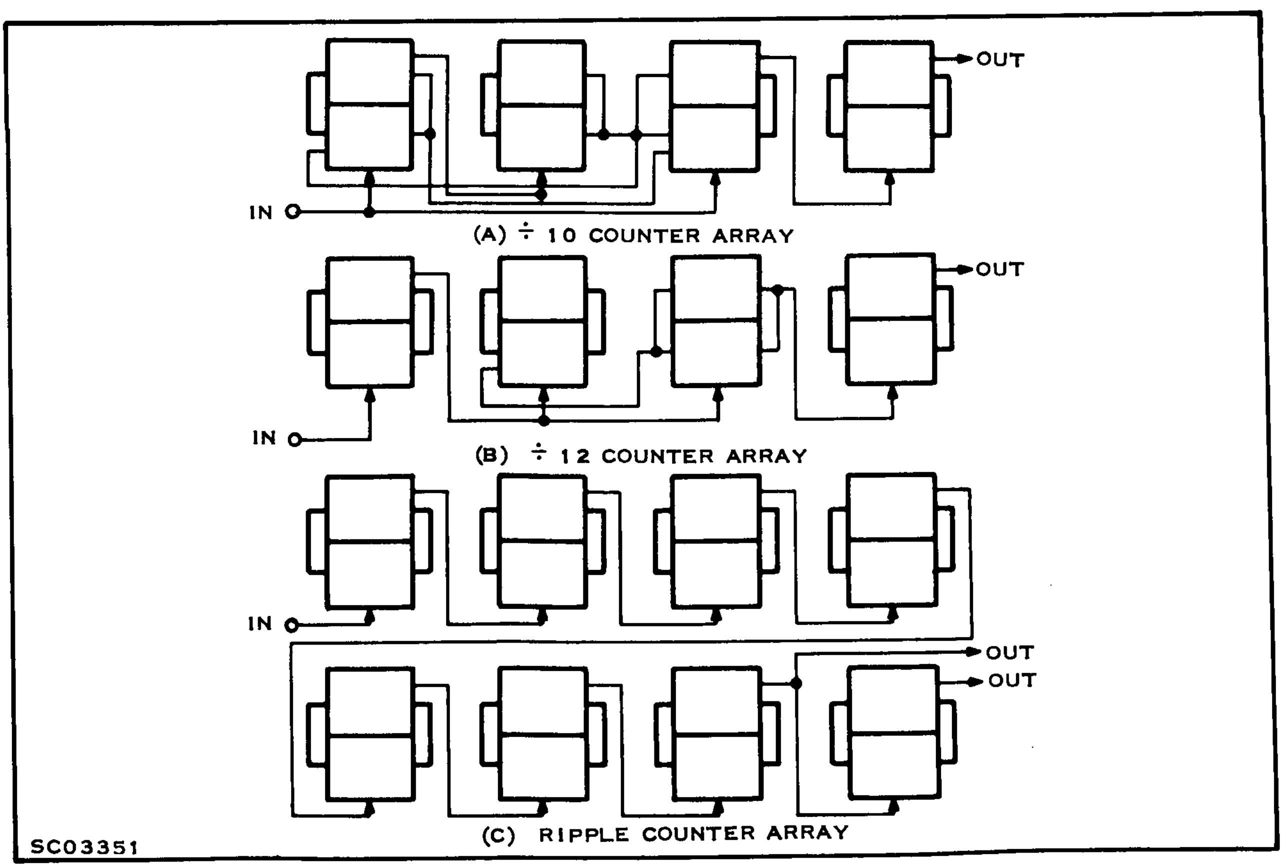


Figure 39. Array Interconnection

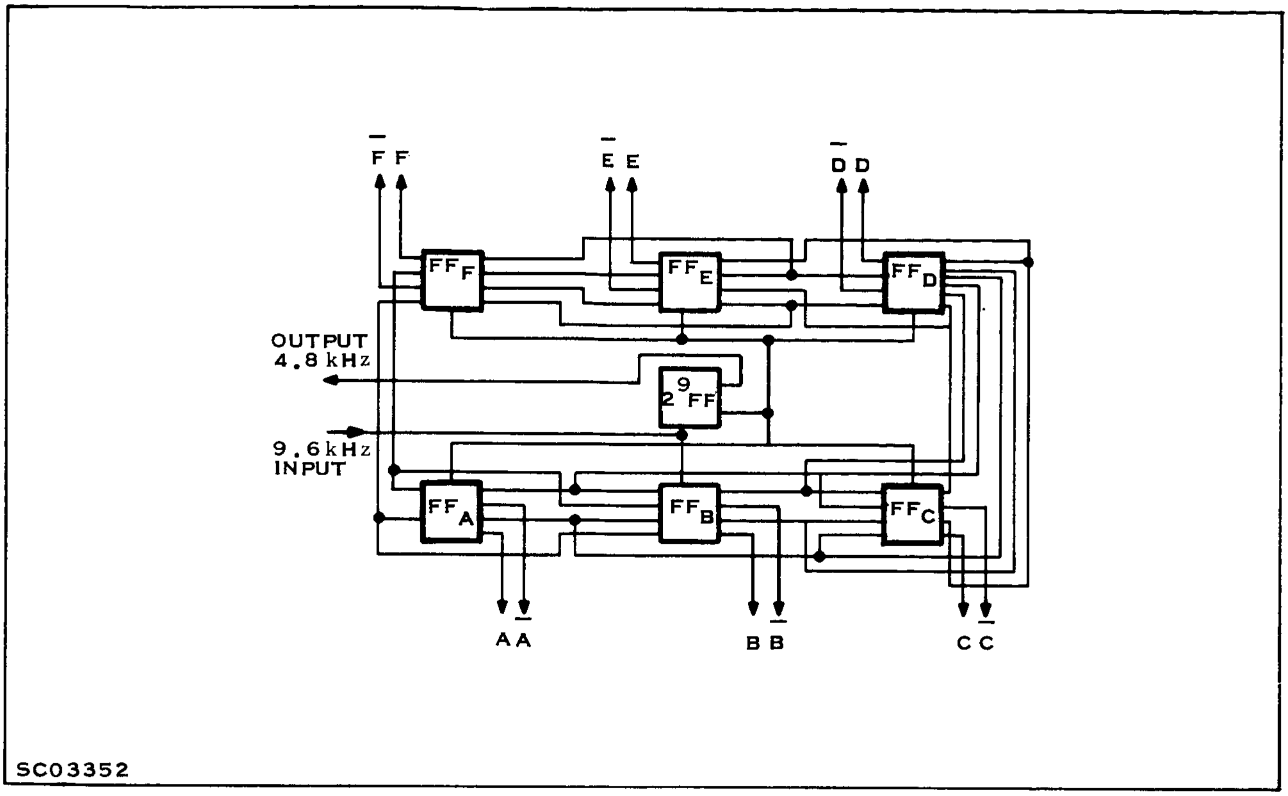


Figure 40. Johnson Counter Block Diagram

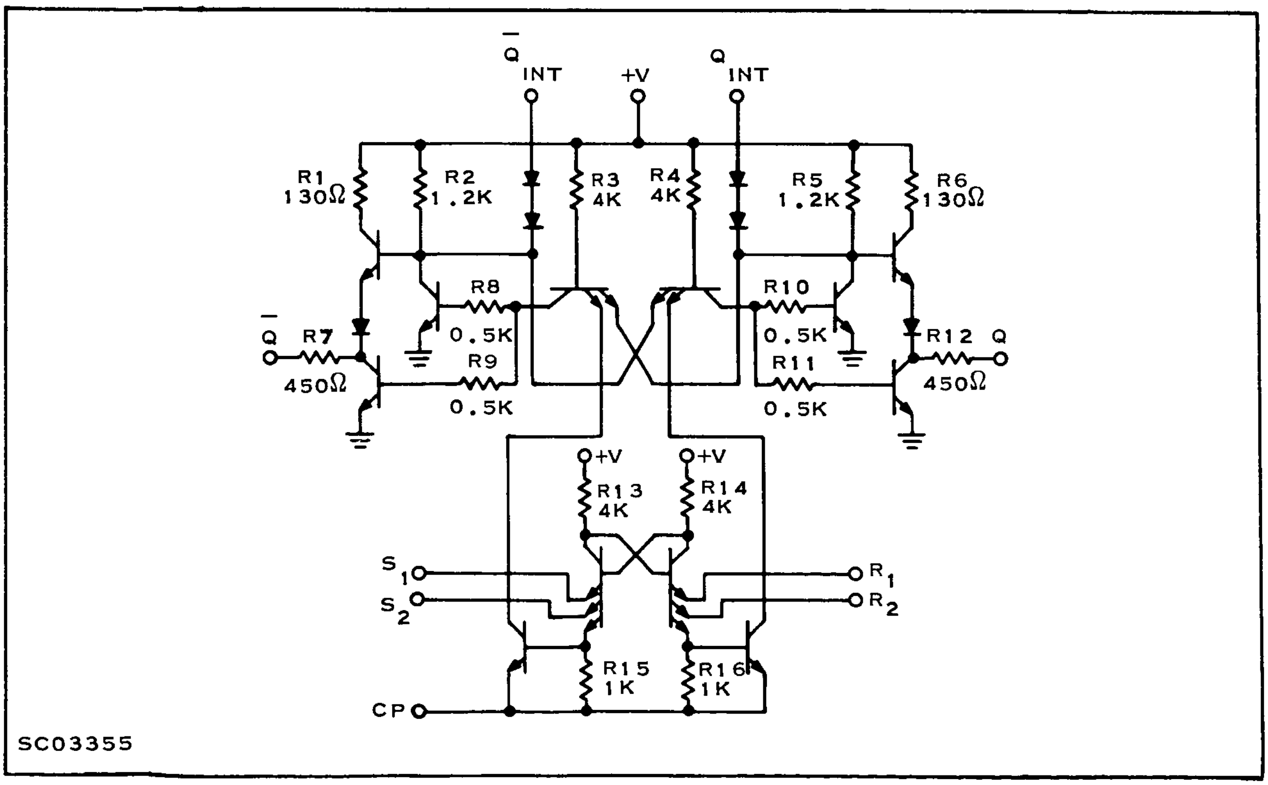


Figure 41. Johnson Counter Flip-flop

B. PACKAGE

Operating temperature range is from -25° to 125°C. A moly-gold metallization system is used for surface interconnections for the arrays, in order to eliminate any possibility of "purple plague."

The package used for these arrays is a modification of a 16-pin package presently in production at Texas Instruments. Due to the large size of silicon die required, it was necessary to invert the ceramic substrate in order to obtain a sufficiently large flat-surface area for mounting (note Figure 42). The silicon is alloyed to the metallized band, using a metallization technique developed by Texas Instruments and used for the first time on this program. A layer of nickel is evaporated on the back of the slice, followed by a layer of silver. The nickel acts as a welting agent to allow the gold plate on the package to wet the silicon during alloying of the silicon chip to the package header.

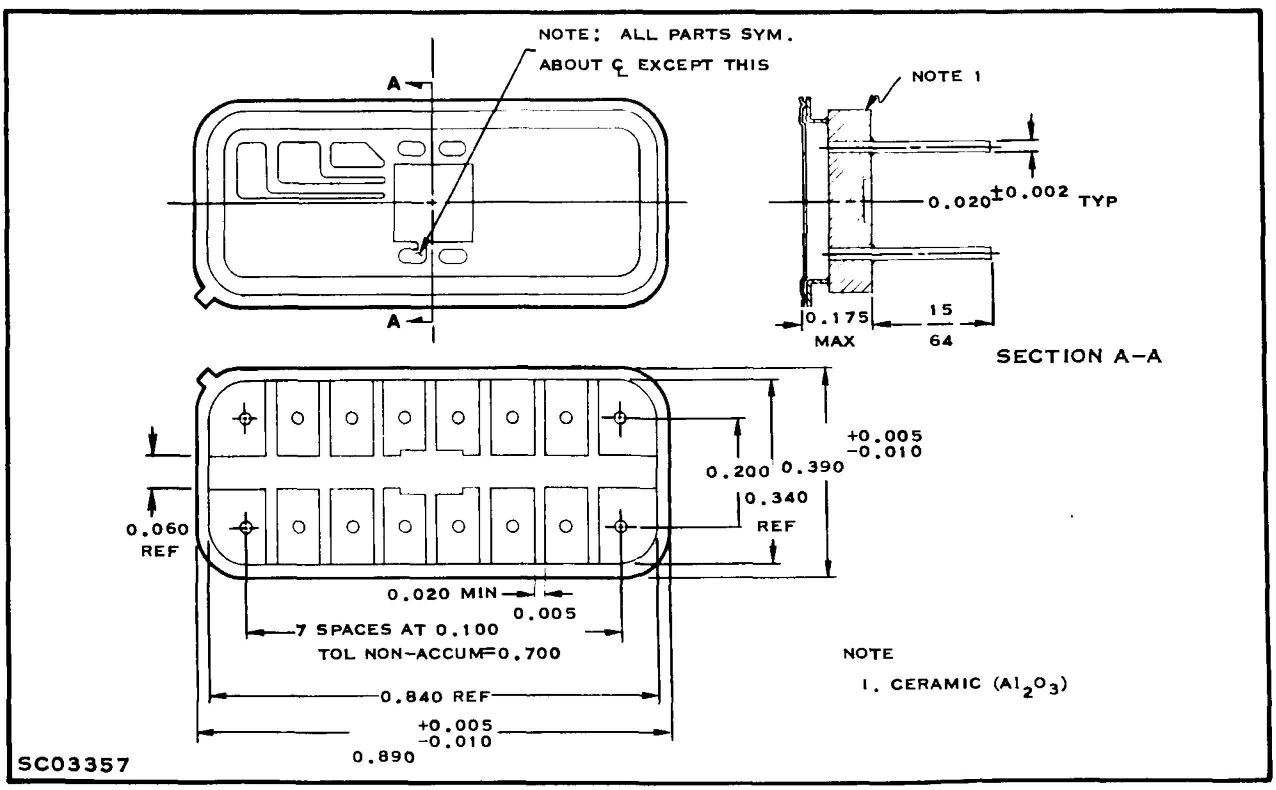


Figure 42. Assembly — Package 75 VA Inverter Array

Silver is used to prevent the nickel from oxidizing. Initially the nickel-silver evaporation was performed before applying the moly-gold metals to the top of the slice. However, where this was done the silicon was exposed where metal contacts were to be made. This exposed silicon reacted with the silver ions, producing poor metal contacts. A technique was then developed for applying nickel-silver metallization after the moly-gold evaporation. This produced an excellent method of assembly for the integrated-circuit chips. Thermal impedances for the Johnson Counter and ripple counter arrays were found to be 0.033C°/mW. The decade and ÷ 12 arrays had thermal impedances of 0.094 C°/mW. The difference in values here is due to the difference in area of the silicon chips involved.

C. RIPPLE COUNTERS

The ÷ 10, ÷ 12, and ÷ 256 arrays use the R-S flip-flop shown above in Figure 38. This circuit utilizes a master flip-flop (controlled by the input logic) to drive a slave flip-flop (which copies the master flip-flop under clock control). Thus, positive anti-race is assured. TTL logic is employed to achieve maximum circuit densities for these arrays. Use of TTL logic for high-density arrays was unique with this program. Since its inception both the Large Scale Integration (LSI) program at Texas Instruments (sponsored by Wright-Patterson Air Development Center) and the Texas Instruments catalog line of arrays have adopted this technique.

A common set of oxide removal masks was used for these three array types, with a different metallization mask for each. Interconnection of the arrays is shown in Figure 39. Note that the eight-stage ripple counter (÷ 256) is really two four-stage counters on a single chip. This essentially produced a four-fold increase in yield for this device, since any given four-stage counter section could be used as either the first or last half-counter, depending on the location of other good four-stage counters adjacent to it on the slice.

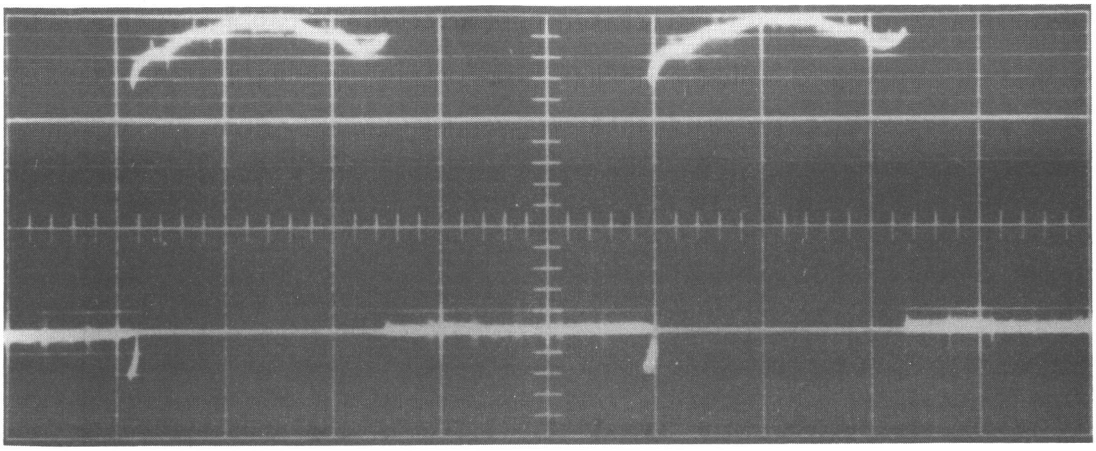
Electrical requirements for these arrays were quite straightforward, and no particularly severe design problems were encountered in their development. Process problems, along with process control of the Johnson Counter array, will be discussed in a later section.

D. JOHNSON COUNTER

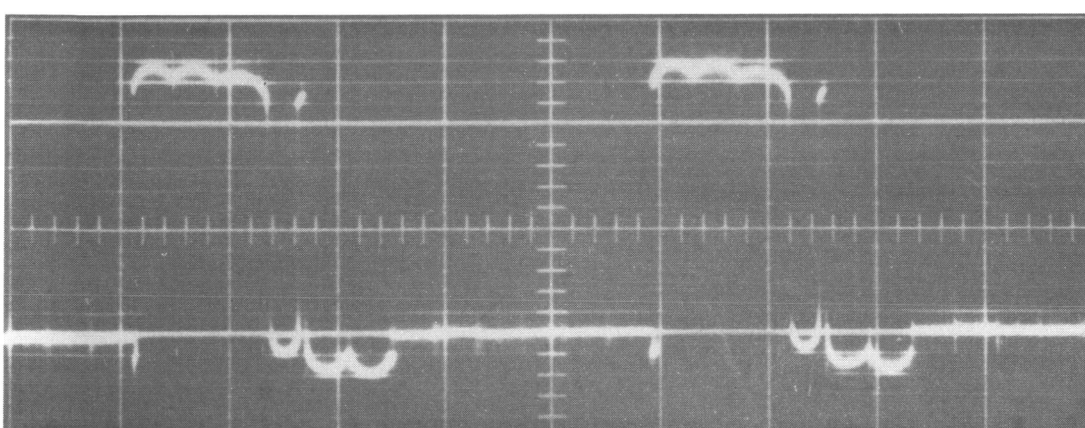
In addition to the requirement that the Johnson Counter circuitry be totally contained on a single monolithic chip, two unique requirements also had to be met by this design. First, the counter was to be self-synchronizing, the synchronization to occur within a maximum of three clock pulses after power turn-on; second, each counter flip-flop must be capable of driving a minimum of 2.5 mA into the base of a power darlington, which could be either 2.2 volts above ground, or actually be close to 0.2 volt below ground, when the Johnson Counter output is supplying current. (See Figure 43, power darlington V_{BE}.)

Considering the application for this system, there can be no provision for a manual preset. Therefore, the logic count had to be internally self-synchronizing. Out of the 64 (2^6) possible states, only 12 are legitimate. Any other combination will produce excessive current in the output transformers, with attendant over-heating. Each of these 12 states can be completely and uniquely defined using only two of the six logical terms available. The switching actions that occur in this counter are indicated in Table III. The algebraic sum of these terms is the 400-Hz sine wave required for the inverter system.

The logic used in this counter is shown in Table IV.



100% RATED LOAD



NO LOAD

SC03356A

Figure 43. Power Darlington V_{BE}

Table III. Counter Sequence

Count Stored	A	B	C	D	E	F	Min-term Logic
0	0	0	0	0	0	0	$\bar{A} . \bar{F}$
1	1	0	0	0	0	0	$A . \bar{B}$
2	1	1	0	0	0	0	$B . \bar{C}$
3	1	1	1	0	0	0	$C . \bar{D}$
4	1	1	1	1	0	0	$D . \bar{E}$
5	1	1	1	1	1	0	$E . \bar{F}$
6	1	1	1	1	1	1	$A . F$
7	0	1	1	1	1	1	$\bar{A} . B$
8	0	0	1	1	1	1	$\bar{B} . C$
9	0	0	0	1	1	1	$\bar{C} . D$
10	0	0	0	0	1	1	$\bar{D} . E$
11	0	0	0	0	0	1	$\bar{E} . F$
0	0	0	0	0	0	0	

Table IV. Logic Control Equations

$t_n + 1$		t_n
a	=	$\bar{A}. \bar{F}$
$\bar{a}$	=	$A. F$
b	=	$A. \bar{B}. \bar{F}$
$\bar{b}$	=	$\bar{A}. B. F$
c	=	$A. B. \bar{C}$
$\bar{c}$	=	$\bar{A}. \bar{B}. C$
d	=	$A. B. C. \bar{D}$
$\bar{d}$	=	$\bar{A}. \bar{B}. \bar{C}. D$
e	=	$C. D. \bar{E}$
$\bar{e}$	=	$\bar{C}. \bar{D}. E$
f	=	$D. E. \bar{F}$
$\bar{f}$	=	$\bar{D}. \bar{E}. F$

Notice the use of additional redundant terms, particularly in the logic for the D flip-flop. These extra control terms are necessary to provide the required self-synchronization capability for the counter. The block diagram for this counter is shown in Figure 40; pin-number assignment for the 16-pin package is seen in Table V.

Table V. Pin Assignment — Johnson Counter Array

Pin No.	Assignment
1	E
2	F
3	$\overline{F}$
4	Ground
5	4.8 kHz out
6	$\overline{A}$
7	A
8	$\overline{B}$
9	B
10	C
11	$\overline{C}$
12	V_{CC}
13	Input
14	$\overline{D}$
15	D
16	$\overline{E}$

A two-step computer program was required for generating the interconnection mask for this array. The array was split into six segments; the computer generated the interconnection pattern for each segment. Then an additional computer program was used for interfacing the six segments to make a composite interconnection pattern.

At the time of this array's development the only suitable materials available as dielectrics for multilevel interconnection were all organic in nature. This, coupled with the relatively poor yield at the time for multilayer metallization, made the use of a single level of metallization quite desirable. This meant that the entire array interconnection was accomplished simultaneously with interconnection of the components of the counter's individual flip-flop.

Ramifications of this approach are several and varied. First, the failure-analysis problem was a continual plague. Since all components of the array are interconnected simultaneously, when a particular array does not operate the cause of failure is completely unknown; i.e., it could be a faulty component, faulty flip-flop, faulty interconnections, or any combination of these. It is extremely difficult to trace a signal through a master-slave J-K flip-flop (which has a total of three closed feedback loops); it is even more difficult to trace a signal through a six-stage folded-ring counter of these flip-flops. This great difficulty is even further compounded by the extra control logic lines used for self-synchronizing. One engineer and one technician would require from one to one and one-half days to locate the point where a signal was lost in this array.

A second ramification of doing all metallization on a single level is the amount of surface area required for metallization. This is a direct factor in yield considerations. If two levels of metallization were used, incorporating technologies which have been developed and proven since inception of this program, it appears that the size of the Johnson Counter array could then be decreased from its present 0.135 x 0.135 inch to approximately 0.070 x 0.100 inch. This is a decrease in area of 62 percent. This by itself would present a seven-fold increase in yield. In addition, by using the first level of metallization to generate individual flip-flop unit cells, the individual flip-flop can be used as any flip-flop in the array.

As a result, arrays could be obtained from areas of a slice that now partially overlap four different arrays. This means that whereas single-level metallization results in a cluster of four arrays, each of which partially operates, two-level metallization would allow the shewing of the portion of the array in order to encompass an "area of goodness" for the entire array. It is readily apparent that the amount of surface area required for single-level interconnection of the array, coupled with the extremely high percentage of surface area which must be flawless (either for device junctions or for metallization), is incompatible with the present state of the art in process control. Coupled with the significant improvements in multilevel interconnection technology during the past year, it is recommended that future arrays of this degree of complexity be designed using multilevel interconnect techniques.

The number of components used in this array is listed in Table VI.

Table VI. Johnson Counter Array-component Count

Components	Count
Transistors	82
Resistors	106
Diodes	42
TOTAL	230

Improvements in photomask resolution and alignment techniques now allow a decrease in horizontal (surface) geometries of devices without deteriorating device quality or yield. In this program, 0.4-mil emitter contacts on 0.8-mil emitters were used; in the future, 0.3-mil contacts on 0.6-mil emitters could just as readily be employed. This technique would also allow a significant reduction (approximately 50 percent) in the surface area required for the array. (This does not include any additional area required by the metallization pattern.)

E. TESTING

The test fixture used for slice probe and assembled device evaluation is shown in Figure 44. This test set was used for all four types of arrays. Equivalent loads were provided for all outputs; equivalent sources were furnished for driving the arrays under test. In addition, oscilloscope monitor points were provided on all inputs and outputs. Notice that in lieu of suitable power darlington devices three conventional (IN914) diodes were used in generating an equivalent V_{BE}.

First test given a circuit is purely functional in nature. The slice is "mapped," giving the locations of good unit cells, or arrays, on the slice. This map then accompanies the slice to the device assembly area, where the slice is scribed and broken apart, and the good chips removed and alloyed into headers. Leads are next ball-bonded from the chip to the package's output pins. The device is then tested electrically at room temperature and at +125° C. Low-temperature testing was performed on capped and sealed units only.

An example of the type of failure which was prevalent in this program is shown in Figure 45.

This type of symptom suggested a parasitic surface phenomon such as oxide pin-holes as the cause of failure; however, when metal was removed from the surface, additional oxide (in the form of TEOS) was deposited on the surface, and it was then remetallized, the leakage actually increased. In this particular case the cause of failure was shown to be epitaxial stacking faults, which produced lattice dislocations at the device junctions.

A more detailed case history of the different lots of material, with microphotographs of the diverse failure modes, is presented in the Supplement, Exhibit C, along with other pertinent information about the Johnson Counter.

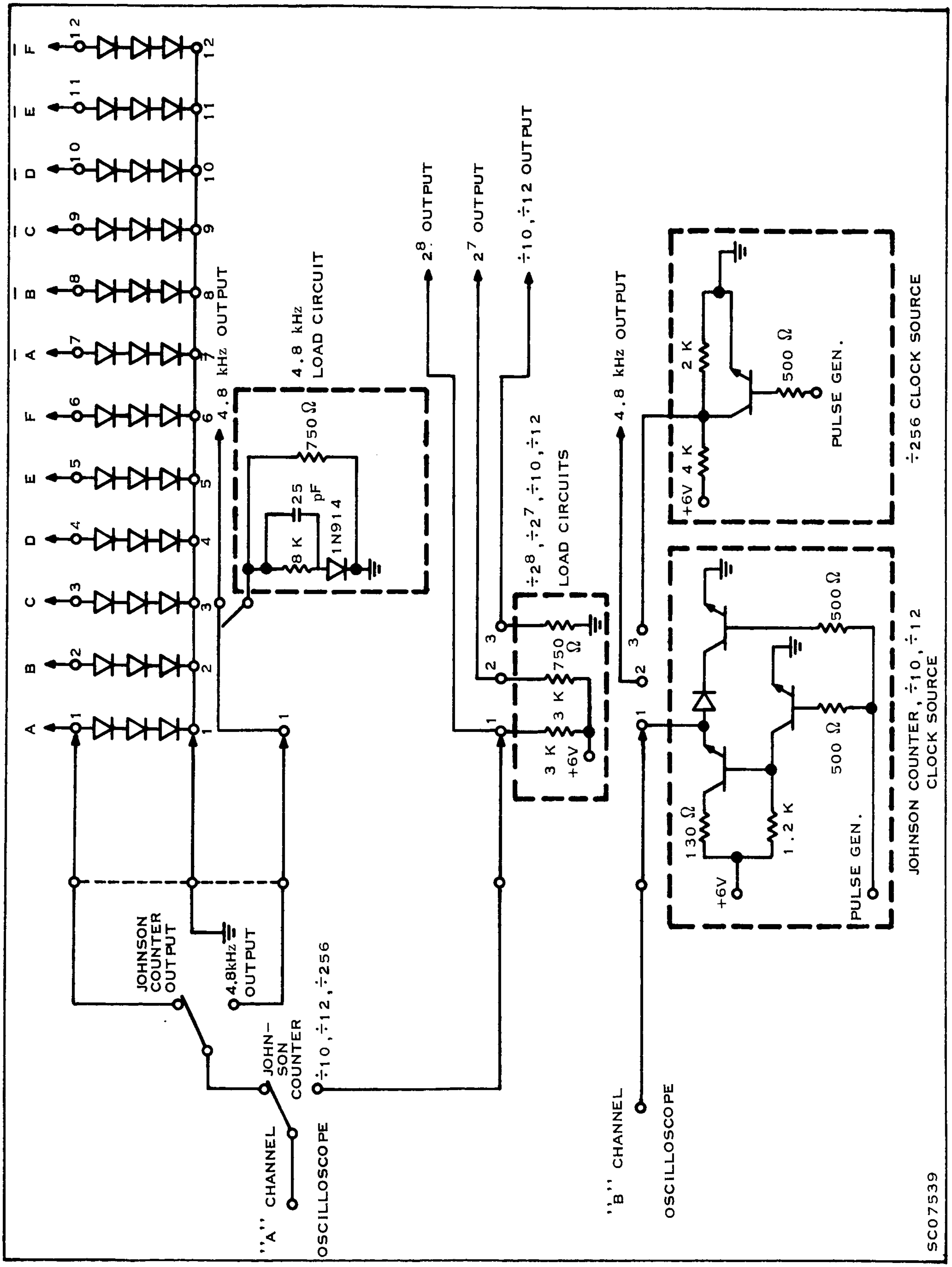


Figure 44. I/C Array Test Fixture

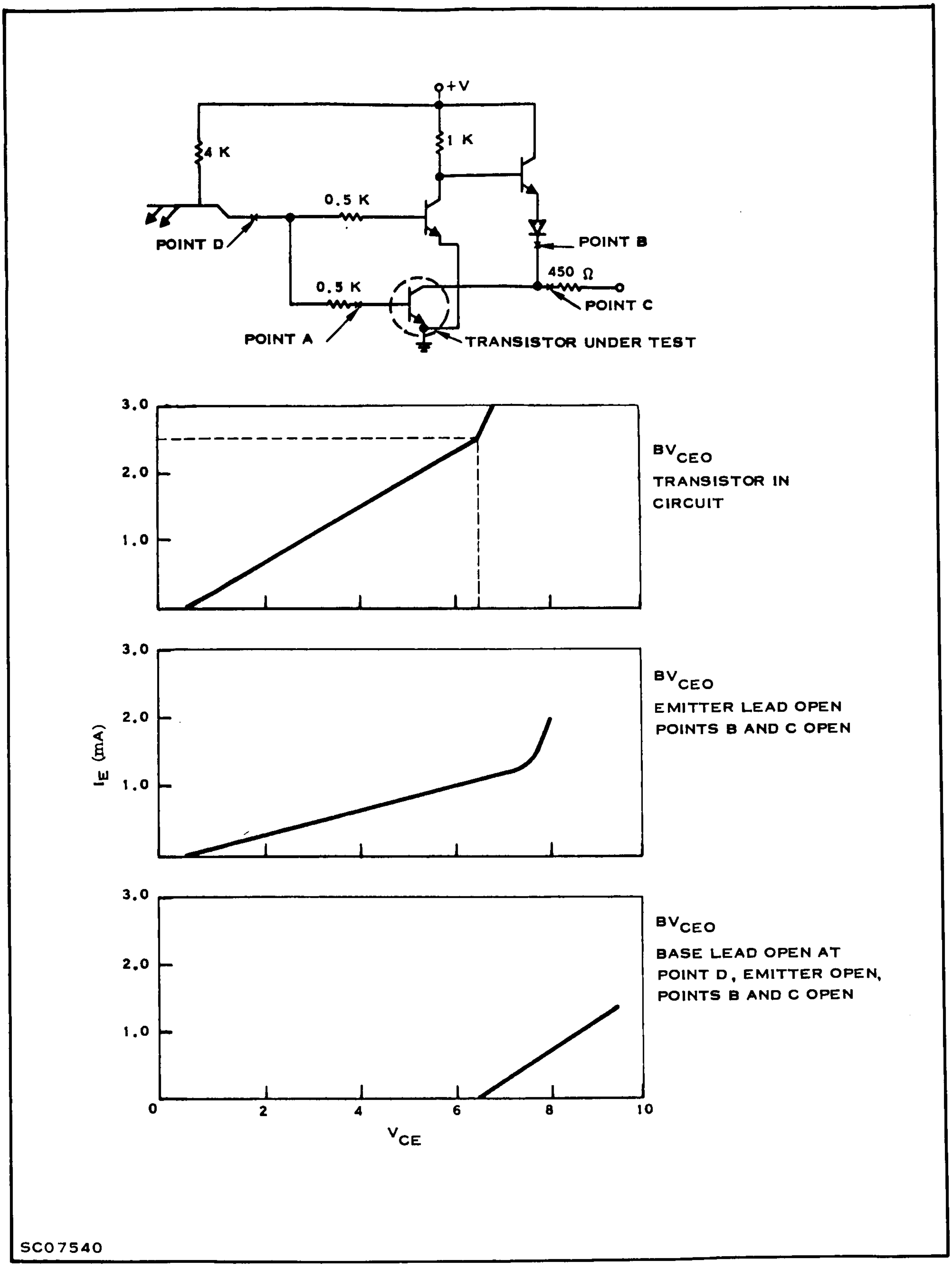


Figure 45. Johnson Counter Output

F. SUMMARY

Out of four array types to be developed and delivered in operational inverter systems, three types were completed which satisfactorily met the specifications. The fourth array, the Johnson Counter, had limited success.

The first lot of Johnson Counter material was completed through metallization on 30 March 1966. This lot of 17 slices yielded 40 operating Johnson Counter arrays at slice probe. Assembly and packaging problems caused the loss of all but six of these arrays. The six arrays were tested in the inverter system at room temperature; two were destroyed due to faulty packages. The remaining four arrays operated in the system under all loads at 25° C. However, excessive leakage currents prevented attaining the specified current from several outputs. This leakage current, it is thought, is due to misalignment during the oxide removal for the emitter contact. This problem should be quickly corrected on ensuing lots of material. A detailed case history of these dots of material is shown in the Supplement, Exhibit C. No additional operating Johnson Counter arrays were obtained until 9 November 1966.

A lot produced on that date yielded a total of 10 arrays which operated partially; i. e., either not all outputs gave proper current and voltage levels, or the count sequence was not correct. One of these arrays that counted properly had 11 of the 12 outputs deliver specified currents and voltages. The $\overline{B}$ output transistor, however, had an oxide smear which prevented the transistor from turning off. This transistor is shown in Figure 46.

This material was processed using the most careful and conservative techniques. Still no operational arrays were obtained, although several dozen were observed that "almost worked." It is therefore apparent that this array design, with the geometries and metallization pattern used, is not a feasible production item; however, as was

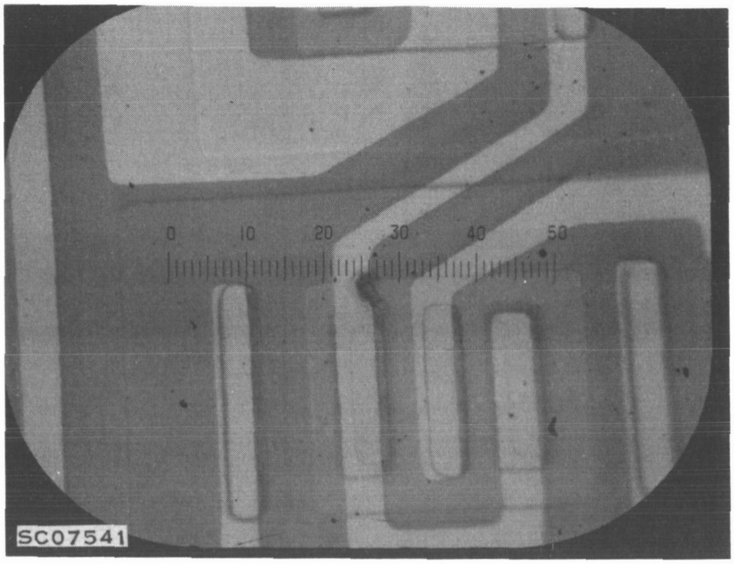


Figure 46. $\overline{B}$ Source XTR

discussed above, an array of this complexity would indeed be feasible using smaller geometries and multilevel interconnections. Both of these techniques are well developed, and at present constitute quite good yield technologies.

SECTION VI

QRA ENVIRONMENTAL TESTING

Due to the relatively small quantity of parts required for the design and development contract on the NASA 75-VA inverter, it was not possible to perform sample testing. To assure device reliability all developmental semiconductors (L-163, L-164, L-166, L-167, L-168, L-169) were subjected to the environmental test conditions specified for subassemblies in the NAS8-11925 RFQ. Additional tests were performed where necessary to verify inverter quality and reliability.

A. TEST SEQUENCE ON SEMICONDUCTORS

1. Hermeticity

a. Radiflo

Radioactive tracer gas (Krypton 85) was used to examine components for fine leaks. The two test ranges employed for components on this program were 1×10^{-6} atm. cc/sec on the L-163, 164, 166, 167, and 168, and 1×10^{-8} atm. cc/sec on L-169.

b. Gross Leak

Ethylene glycol was heated to 105° C. Devices were immersed in the solution and observed for emission of bubbles to detect hermetic-seal leaks greater than 1×10^{-6} atm. cc/sec.

2. Temperature Cycling

Temperature extremes of +125° C and -55° C were used. All tests consisted of five cycles, with 30 minutes of exposure at the extreme and 10 seconds transfer time.

3. Mechanical Shock

Each semiconductor was subjected to 500 g 1.0 millisecond half-sine shock pulse to determine mechanical integrity of internal construction. Orientation and number of impacts per axis were Y_1, Y_2, X_1, and Z_1 axes and five (5) impacts per axis.

4. Sinusoidal Vibration

Stress level of 0.5 inch displacement 10 - 28 Hz 20 g acceleration 28 - 2000 Hz was performed on each device for one four-minute frequency sweep in each of three mutually perpendicular axes. The purpose of this test is to assure that no destructive resonance will be excited during exposure to the above frequency range and stress level.

5. Constant Acceleration

Each device was subjected to 100 g for one minute in each of the six (6) axes X_1, X_2, Y_1, Y_2, Z_1, and Z_2. This test validates mechanical integrity through assuring proper bond strength.

6. Hermeticity

Same as Step 1.

7. <u>Radiographic Inspection</u>

Each device was subjected to X-ray to assure that no extraneous matter or faulty workmanship exists in parts.

8. <u>Vibration Test on Complete Inverter</u>

Two complete inverter systems were subjected to 3 g 20-2000 Hz for one six-minute frequency sweep in each of three (3) mutually perpendicular axes while operating.

B. SUMMARY

From the standpoint of mechanical integrity the development semiconductors exhibited essentially the same characteristics as present power and integrated-circuits parts.

SECTION VII
SYSTEM PACKAGING

A. GOALS AND RESULTS

1. Reliable Operation

Reliable operation was considered a major goal. The objective was to design a package free of possible structural or electrical failure, resonance, or similar deficiencies which could cause significant changes in the unit's characteristics.

2. Maximum Serviceability

Another of the goals in this design concept was maximum serviceability.

3. Minimum Size and Weight

Another design goal was minimum size and weight consistent with good design practice and with contractual reliability standards.

4. Modern Techniques

Use of modern techniques and standard, readily available parts was a requirement self-imposed by the designers to hasten development.

Modular construction with maximum use of etched circuitry was employed. After the schematic was separated into functional divisions, these divisions were further reduced into groups of components or elements which would facilitate production and would permit replacement of relatively inexpensive units rather than necessitate repair of expensive plug-in components. The design had to accommodate two different component arrangements:

a) Component groups similar in physical configuration which were repeated in the circuit.

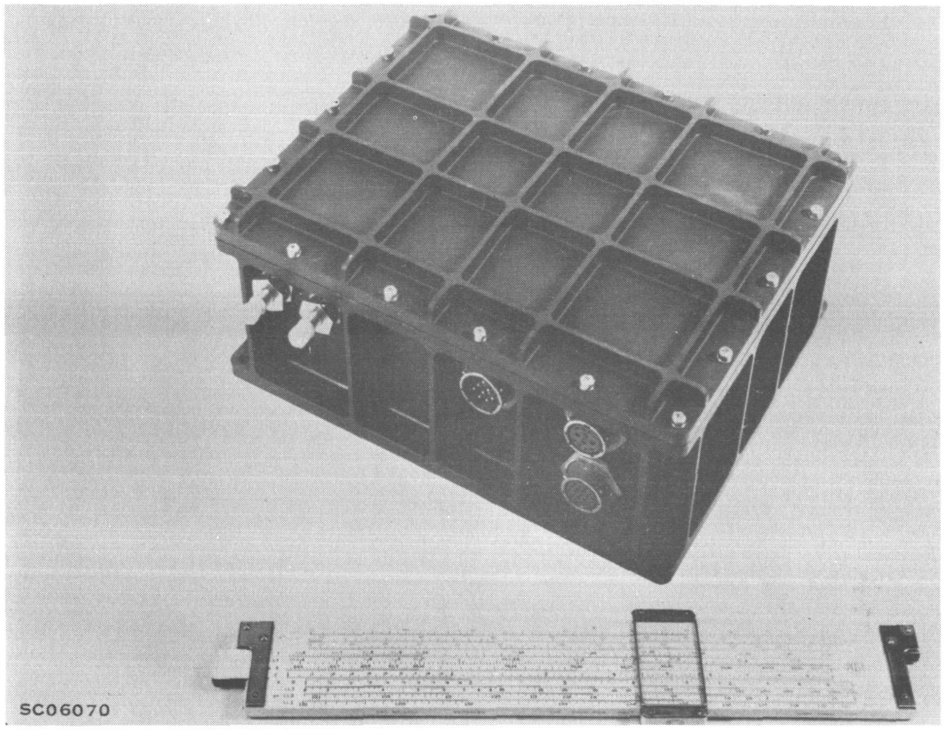
b) Component groups which were dissimilar and not repetitive.

5. Approach

A review of the circuit suggested the feasibility of a functional division into a convenient number of subcircuits. These subcircuits were designated as the Potted Assembly of Power Transformers, PA-1; Potted Assembly of DC Filter Capacitors, PA-2; Potted Assembly of AC Inductors, PA-3; Potted Assembly of DC Filter Chokes, PA-4; Low-level Circuitry P.C. Board, and Johnson Counter P.C. Board.

Fabrication details of these subassemblies as well as all case and system packaging drawings are presented in the Supplement, Exhibit D.

This circuit breakdown and division yielded additional benefits in the form of subcircuits which could be individually advanced toward prototypes. These could be substituted in the original breadboard to verify performance toward the original design in relation to the overall circuit. Once the detailed design concept of the subcircuits was established, conversion to a physical unit followed very closely. Figure 47 shows photographs of the finished inverter.



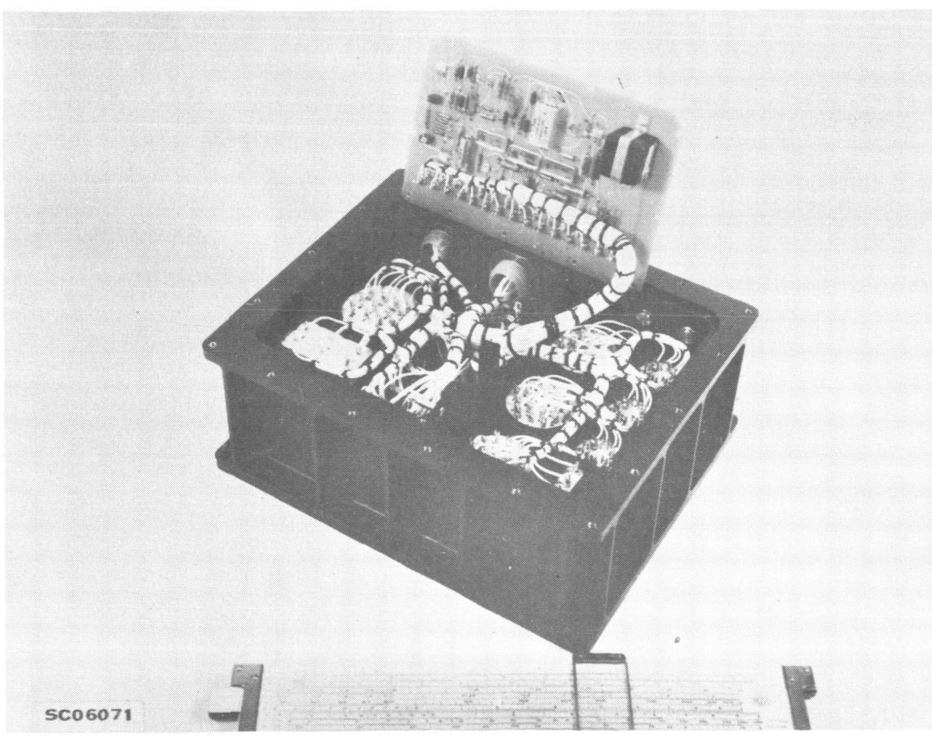


Figure 47. 75-VA Static Inverter

B. HISTORY: JUSTIFICATION OF PRESENT DESIGN

The outer case was constructed to withstand the environmental specifications stated in the System Description section. The hard, black anodized finish was selected to withstand external abuse and provide the greatest amount of thermal radiation. The bottom surface, which is in contact with the "cold plate," has a chromate finish to insure good thermal conduction as well as maximum electrical conductivity for the case ground.

Transformer and capacitor housings were constructed to withstand the previously mentioned environmental specifications. Their shape was dictated by the modular construction objective as well as by trying to maintain as small a dimension as possible in the X and Y axes. As the Z axis increased on the various housings, so did their susceptibility to the mechanical environment. Coupled with this was a desire to have each assembly self-supporting as far as contact with the X-Y axis was concerned.

Also included in the design criteria was the possibility of mass production, in which case the housings could easily be cast or machined. These are finished in a hard, black anodize, which provides a durable finish against abuse and also a good radiant-heat transfer. Hard anodizing provides high-quality electrical isolation of the internal components from the case-ground potential. A simple, light, strong case was the result.

The printed circuit boards were designed to nest over the transformers and their cabling. Tallest components on the boards were designed to mount over the areas where the shortest transformer housings and the least amount of cabling were required. The material's type, thickness, and finish were selected on the basis of strength, durability, and the variety of assembly techniques.

The internal layout is based on many factors, one being susceptibility to radiation, magnetic, audio, and radio frequencies. Another factor was radiated interference to other equipment. Care was taken to protect internal functions from being upset by other internal signals. Each component had its own separate thermal characteristics, which required for some a means for effective thermal dissipation.

NASA had specified a certain external mounting-hole pattern as well as a minimum length, width, and depth. A correlation of all of the above-cited factors, coupled with a practical approach toward manufacturing, cost, and quality control, led to the final layout.

SECTION VIII

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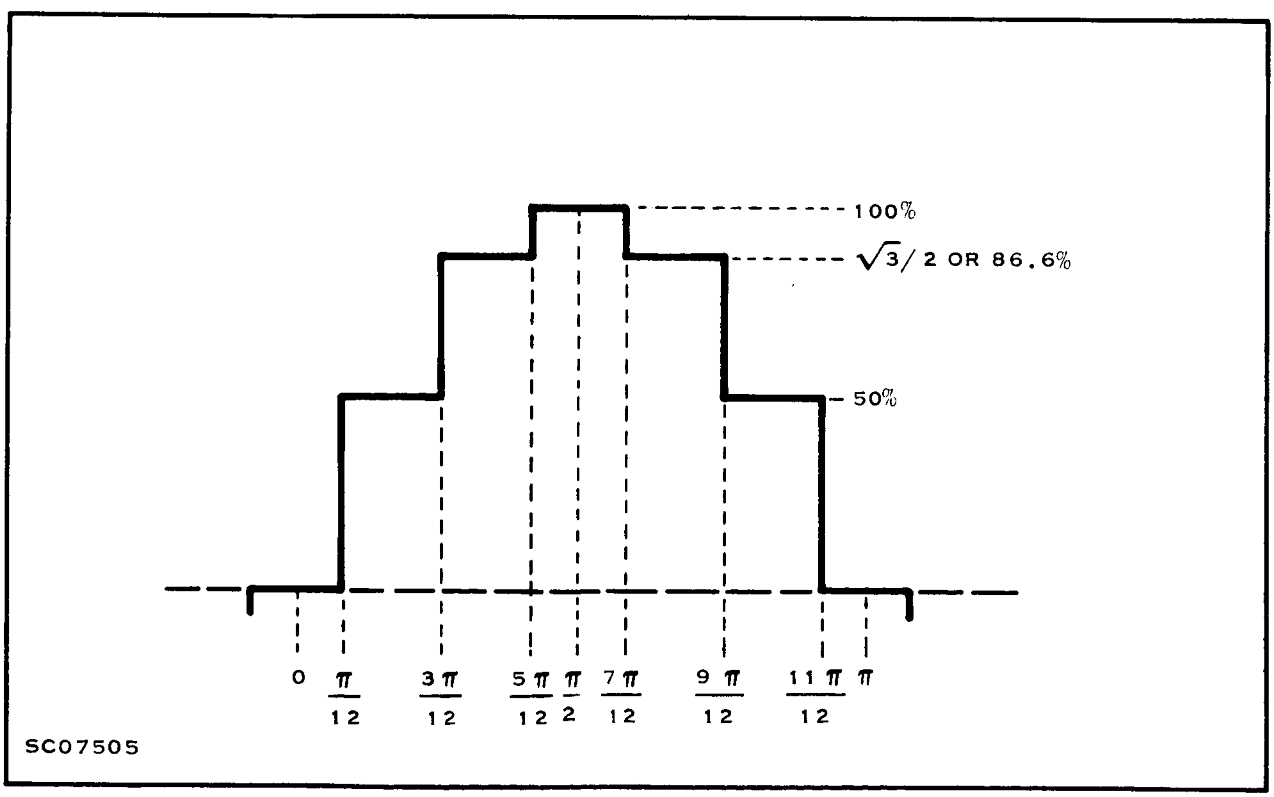
APPENDIX A

IDEAL STEP-APPROXIMATED WAVESHAPE

APPENDIX A

IDEAL STEP-APPROXIMATED WAVESHAPE

The ideal step-approximated waveshape seen below can be shown by Fourier analysis to contain no harmonics below the 11th.



Ideal Step-approximated Waveshape

APPENDIX B

Parts List—75-VA Static Inverter

Component Designations — Refer to Figure 7 in Main Report

Component Designation	Description of Components	Manufacturer	Comments
Q1-Q7	L-163, Dual-power NPN Darlington Transistor, 6-Pin Stud Package	TI	Developmental Item
Q8	L-164, Dual-power NPN-PNP Transistor, 6-Pin Stud Package	TI	Developmental Item
G1	G1, Isolated Common Terminal	TI	Developmental Item
D1	1N3890, 100V, 12-Amp Fast-Recovery Rectifier, DO-4 Type Package	TI	
C4-C6	K1G333K- 2, .033 uf, 100 VDC, ± 10% Polycarbonate Capacitor	Elpac	
C7-C8	186P33491T15, .33 uf, 100 VDC, ± 10% Metal Clad Capacitor	Sprague	
X1	G-663 Thermistor (NASA Part #50M10346)	FEIC	
M4	PA-2, Potted DC Filter Capacitor Assembly C9 202D108X0050A5, 50 VDC, 1000 uf ± 20%, Sprague Tantalum Capacitor C10 202D357X9150A5, 150 VDC, 350 uf ± 10%, Sprague Tantalum Capacitor C11 202D198X9015A2, 15 VDC, 1900 uf ± 10%, Sprague Tantalum Capacitor	TI	Developmental Item
M1, M2, M3	Pa-1, Potted Power Transformer Assembly Two Transformers: Cores-Magnetics Inc. 52026-2S Tape-Wound Toroids, PR1. 180T, SEC. NS1 = 120T, NS2 = 90T, NS3 = 30T. All wire is No. 23 H.F.	TI	Developmental Item

Component Designations (Continued)

Component Designation	Description of Components	Manufacturer	Comments
M5, M6, M7	PA-3, Potted Inductor Assembly One AC Choke 1 mh, 63 Turns, #18 H.F. Core: Magnetics 55927-M4 Powdered-Iron Toroid One Voltage Sense Transformer Core: Magnetics 52176-2A, Tape-Wound Toroid, PR1. 900T #36 H.F., SEC. 200T, #34 H.F. One Current Sense Transformer Core: Magnetics 52000-2A Tape-Wound Toroid PR1. 2T #16 H.F., SEC. 500T, #32 H.F.	TI	Developmental Item
M8	PA-4, Potted DC Choke Assembly L-4 ≈ .265 mh, 41 Turns, #13 H.F. Core: Arnold W110168-3 Powdered-Iron Toroid L-5 ≈ .8 mh, 54 Turns, #13 H.F. Core: Arnold W-108281-3 Powdered-Iron Toroid	TI	Developmental Item
M9	PA-5, Potted AC Filter Capacitor Assembly 3 Capacitors: C_1, C_2, C_3. K1H205J-1, 2 uf, 100 VDC, ± 5% Elpac Polycarbonate Capacitors	TI	Developmental Item

Low-level Circuitry P.C. Board

Component Designation	Description of Components	Manufacturer	Comments
TXCO	X-1617706-1, 2.4576 mc Temperature-Compensated Crystal Oscillator	Bendix	Developmental Item
NA1	L-166, Integrated-circuit 8-Stage Ripple Counter Array	TI	Developmental Item
NA3	L-168, Integrated Circuit ÷ 10 Flip-flop Array	TI	Developmental Item
NA4	L-167, Integrated Circuit ÷ 12 Flip-flop Array	TI	Developmental Item
N1	L-169, Integrated-circuit Variable-duty-cycle One-shot; Mask Modification of SN5380	TI	Developmental Item
N2	SN523A, Integrated-circuit Differential Amplifier	TI	
Q9	2N3838, Dual PNP-NPN Transistors in TO-89 Package	TI	
Q10	2N3044, Dual NPN Transistors in TO-89 Package	TI	
Q11-Q13	2N3038, Transistors in TO-50 Type Package	TI	
C16	SCM396BP010C2, 39 uf, 10 VDC, ± 10%, Tantalum Capacitor	TI	
C13	SCH06F221M, 220 pf, 200 VDC, ± 20%, Ceramic Capacitor	Scionics	
C14	K6G563G-G1, .056 uf, 600 VDC, ± 2%, Polycarbonate Capacitor	Elpac	
C15	SCM227HP010D2, 220 uf, 10 VDC, ± 10 %, Tantalum Capacitor	TI	
C17	SCM335FP015A4, 3.3 uf, 15 VDC, ± 20%, Tantalum Capacitor	TI	

Low-level Circuitry P.C. Board (Continued)

Component Designation	Description of Components	Manufacturer	Comments
C18	SCM685BP035D2, 6.8 uf, 35 VDC, ± 10%, Tantalum Capacitor	TI	
Z1	1 %, 1N753, 6.2 V, Breakdown Diode, Moly/G Glass Package	TI	Selected from 1N753 Family
Z2, Z5	1 %, 1N752, 5.6 V, Breakdown Diode, Moly/G Glass Package	TI	Selected from 1N752 Family
Z3	1N969B, 22 V, 2% Breakdown Diode, Moly/G Glass Package	TI	Selected from 1N969B Family
D2, D3, D4 D10, D11, D12	TI-252, 50 V, 40 mA Diffused-silicon Mesa Diode, Micro/G Package	TI	
D7, D8	G130 Stabistor, Silicon Forward-conductance Diode, Moly/G Glass Package	TI	
D9	G129 Stabistor, Silicon Forward-conductance Diode, Moly/G Glass Package	TI	
DA1	TIXD29, 30 V, Dual 10 Array, TO-84 Type Package	TI	
R1-R3	RW59G331, 330 Ω, 3 W, Wirewound Resistor	OMI	
R4-R6	CR-1/8, 442 Ω, 1/8 W, 1 %, Carbon Film Resistor	TI	
R7	CR-1/8, 143 Ω, 1/8 W, 1%, Carbon Film Resistor	TI	
R8	CR-1/8, 750 Ω, 1/8 W, 1 %, Carbon Film Resistor	TI	
R9, R10	3260H-1-101, 100 Ω, Trimpot	Bourns	

Low-level Circuitry P.C. Board (Continued)

Component Designation	Description of Components	Manufacturer	Comments
R11	CR-1/4, 150 Ω, 1/4 W, 1 %, Carbon Film Resistor	TI	
R12	CR-1/4, 200 Ω, 1/4 W, 1 %, Carbon Film Resistor	TI	
R13	CR-1/8, 100 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R14	CR-1/8, 150 Ω, 1/8 W, 1 %, Carbon Film Resistor	TI	
R15, R20, R21	CR-1/8, 3.92 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R16	CR-1/8, 4.99 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R17	CR-1/8, 2.74 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R18	CR-1/8, 14.3 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R19	MC65 T-2, 309 Ω, 1/2 W, 1 %, Metal Film Resistor	TI	
R22	MC65 T-2, 953 Ω, 1/2 W, 1 %, Metal Film Resistor	TI	
R23	CR-1/8, 10 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R24	CR-1/8, 2.05 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R25	CR-1/2, 5.23 K, 1/2 W, 1 %, Carbon Film Resistor	TI	
R26	RW69V102, 1 K, 3 W, Wirewound Resistor	Sprague	
R27	CR-1/8, 3.01 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R28	CR-1/4, 825 Ω, 1/4 W, 1 %, Carbon Film Resistor	TI	

Low-level Circuitry P.C. Board (Continued)

Component Designation	Description of Components	Manufacturer	Comments
R29	820 Ω, ± 2 %, TI-1/4, Sensitor	TI	
R30	CR-1/8, 121 Ω, 1/8 W, 1 %, Carbon Film Resistor	TI	
R31, R34	CR-1/8, 1.02 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R32, R33	330 Ω, ± 5 %, TM-1/8, Sensistor	TI	
R35	CR-1/8, 82.5 K, 1/8 W, 1 %, Carbon Film Resistor	TI	
R36	CR-1/4, 665 Ω, 1/4 W, 1 %, Carbon Film Resistor	TI	
	Johnson Counter P.C. Board		
C12	SCM396BP010C2, 39 uf, 10 VDC, ± 10 %, Tantalum Capacitor	TI	
R37-R48	CR-1/8, 543 Ω, 1/8 W, 1 %, Carbon Film Resistors	TI	
N3	SN5311 Dual 5 Input NAND Gate	TI	
N4	SN5300 J-K Flip-flop	TI	
N5-N7	SN5302 Dual J-K Flip-flops	TI	

APPENDIX C

75-VA INVERTER TEST DATA

75 VA INVERTER TEST DATA

DATE 11-29-66 UNIT UNDER TEST 1001 DATA BY L. J. B. AMBIENT TEMP. -25°C

VIN \ PO	(NO LOAD) 0%	(27Ω) 100%	(18Ω) 150%	(5Ω) Overload	Balanced Short Circuit
25 VDC	VAB 26.3 VBC 26.3 VCA 26.25	VAB 26.2 VBC 26.1 VCA 26.15	VAB 26.0 VBC 25.95 VCA 26.0	VAB 7.5 VBC 7.5 VCA 7.5	
28 VDC	VAB 26.25 VBC 26.25 VCA 26.2 Iin .67A η — D*	VAB 26.1 VBC 26.05 VCA 26.05 Iin 4.08A η 66.1% D* J.C. Vce=4.67	VAB 26.0 VBC 26.0 VCA 26.0 Iin 6.00A η 67% D*	VAB 7.5 VBC 7.5 VCA 7.5 Iin 3.13A η 38.5% D*	Iin 1.83A
30 VDC	VAB 26.3 VBC 26.3 VCA 26.3	VAB 26.25 VBC 26.2 VCA 26.25	VAB 26.0 VBC 26.0 VCA 26.0	VAB 7.55 VBC 7.55 VCA 7.55	

PULSE TRAIN OUTPUT DUTY CYCLES:

4.8 KHZ 49 %

1.92 KHZ 49.5 %

1.6 KHZ 50 %

D* is Distortion Factor Measured with a H.P. Distortion Analyzer in Conjunction with A TRMS Voltmeter

VISUAL OPERATIONAL TESTS

	28V	25V	30V
Turn on & off into No Load - Repeat several times.	✓	✓	✓
Apply balanced short & remove it into a balanced No Load condition - Repeat several times.	✓	✓	✓
Switch to 150% load, turn inverter on & off several times.	✓	✓	✓
Switch to a balanced short circuit, turn inverter on & off several times (observe input DC current).	✓	✓	✓
Switch to unbalanced overload, two phases open, third shorted, turn on & off several times (observe open phase)	✓	✓	✓
Switch to 100% load, short one phase; remove short.	✓	✓	✓
Switch to 150% load, short one phase; remove short.	✓	✓	✓
Turn on into inductive load-Repeat several times, do same at each of other two input voltages	✓	✓	✓
Connect up continuously varying load & vary it throughout its complete range; repeat several times. Then do same at each of other two input voltages.	✓	✓	✓
Check pulse train outputs for correct frequency & duty cycle	✓	✓	✓

75 VA INVERTER TEST DATA

DATE 11-29-66 UNIT UNDER TEST 1001 DATA BY L. J. B. AMBIENT TEMP. +25°C

VIN \ RO	(NO LOAD) 0%	(27Ω) 100%	(18Ω) 150%	(5Ω) Overload	Balanced Short Circuit
25 VDC	VAB 26.15 VBC 26.1 VCA 26.1	VAB 26.0 VBC 26.0 VCA 26.0	VAB 25.8 VBC 25.75 VCA 25.8	VAB 7.5 VBC 7.5 VCA 7.5	
28 VDC	VAB 26.15 VBC 26.15 VCA 26.15 Iin .65A η — D*	VAB 26.0 VBC 26.0 VCA 26.0 Iin 4.02A η 66.5% D* JC Vcc=4.12	VAB 25.9 VBC 25.9 VCA 25.9 Iin 6.00A η 66.5% D*	VAB 7.5 VBC 7.5 VCA 7.5 Iin 3.12A η 37.6% D*	Iin 1.22A
30 VDC	VAB 26.15 VBC 26.15 VCA 26.15	VAB 26.0 VBC 26.0 VCA 26.0	VAB 25.4 VBC 25.85 VCA 25.9	VAB 7.5 VBC 7.5 VCA 7.5	

PULSE TRAIN OUTPUT DUTY CYCLES:

4.8 KHZ 48%

1.92 KHZ 49%

1.6 KHZ 49%

D* is Distortion Factor Measured with a H.P. Distortion Analyzer in Conjunction with A TRMS Voltmeter

VISUAL OPERATIONAL TESTS

	28V	25V	30V
Turn on & off into No Load - Repeat several times.	✓	✓	✓
Apply balanced short & remove it into a balanced No Load condition - Repeat several times.	✓	✓	✓
Switch to 150% load, turn inverter on & off several times.	✓	✓	✓
Switch to a balanced short circuit, turn inverter on & off several times (observe input DC current).	✓	✓	✓
Switch to unbalanced overload, two phases open, third shorted, turn on & off several times (observe open phase)	✓	✓	✓
Switch to 100% load, short one phase; remove short.	✓	✓	✓
Switch to 150% load, short one phase; remove short.	✓	✓	✓
Turn on into inductive load-Repeat several times, do same at each of other two input voltages	✓	✓	✓
Connect up continuously varying load & vary it throughout its complete range; repeat several times. Then do same at each of other two input voltages.	✓	✓	✓
Check pulse train outputs for correct frequency & duty cycle	✓	✓	✓

75 VA INVERTER TEST DATA

DATE 11-29-66 UNIT UNDER TEST 1001 DATA BY L. J. B. AMBIENT TEMP. 125 °C

R / VIN	(NO LOAD) 0%	(27ΩΔ) 100%	(18ΩΔ) 150%	(5ΩΔ) Overload	Balanced Short Circuit
25 VDC	VAB 26.0 VBC 25.95 VCA 25.95	VAB 25.8 VBC 25.75 VCA 25.8	VAB 25.6 VBC 25.55 VCA 25.55	VAB 7.55 VBC 7.5 VCA 7.55	
28 VDC	VAB 26.0 VBC 25.95 VCA 25.95 Iin .65A η — D*	VAB 25.9 VBC 25.8 VCA 25.85 Iin 4.18A η 63.5% D* J.C. Vca=3.60	VAB 25.65 VBC 25.6 VCA 25.65 Iin 6.31A η 64% D*	VAB 7.55 VBC 7.55 VCA 7.55 Iin 3.60A η 33.9% D*	Iin 2.25A
30 VDC	VAB 26.05 VBC 26.0 VCA 26.0	VAB 25.9 VBC 25.8 VCA 25.9	VAB 25.7 VBC 25.65 VCA 25.7	VAB 7.55 VBC 7.55 VCA 7.55	

PULSE TRAIN OUTPUT DUTY CYCLES:

4.8 KHZ 48%

1.92 KHZ 49%

1.6 KHZ 49.5%

D* is Distortion Factor Measured with a H.P. Distortion Analyzer in Conjunction with A TRMS Voltmeter

VISUAL OPERATIONAL TESTS

	28V	25V	30V
Turn on & off into No Load - Repeat several times.	✓	✓	✓
Apply balanced short & remove it into a balanced No Load condition - Repeat several times.	✓	✓	✓
Switch to 150% load, turn inverter on & off several times.	✓	✓	✓
Switch to a balanced short circuit, turn inverter on & off several times (observe input DC current).	✓	✓	✓
Switch to unbalanced overload, two phases open, third shorted, turn on & off several times (observe open phase)	✓	✓	✓
Switch to 100% load, short one phase; remove short.	✓	✓	✓
Switch to 150% load, short one phase; remove short.	✓	✓	✓
Turn on into inductive load-Repeat several times, do same at each of other two input voltages	✓	✓	✓
Connect up continuously varying load & vary it throughout its complete range; repeat several times. Then do same at each of other two input voltages.	✓	✓	✓
Check pulse train outputs for correct frequency & duty cycle	✓	✓	✓

75 VA INVERTER TEST DATA

DATE 12-27-66 UNIT UNDER TEST 1003 DATA BY L. J. B. AMBIENT TEMP. -25°C

P_O / VIN	(NO LOAD) 0%	(27Ω∆) 100%	(18Ω∆) 150%	(5Ω∆) Overload	Balanced Short Circuit
25 VDC	VAB 26.3 VBC 26.35 VCA 26.35	VAB 26.2 VBC 26.25 VCA 26.25	VAB 26.0 VBC 26.05 VCA 26.05	VAB 7.6 VBC 7.6 VCA 7.6	
28 VDC	VAB 26.4 VBC 26.45 VCA 26.45 Iin .602A η — D*	VAB 26.3 VBC 26.3 VCA 26.3 Iin 4.07A η 67.4% D*	VAB 26.1 VBC 26.15 VCA 26.15 Iin 6.11A η 66.5% D*	VAB 7.6 VBC 7.6 VCA 7.6 Iin 3.13A η 39.6% D*	Iin 1.77A
30 VDC	VAB 26.4 VBC 26.4 VCA 26.4	VAB 26.3 VBC 26.3 VCA 26.3	VAB 26.1 VBC 26.15 VCA 26.15	VAB 7.6 VBC 7.6 VCA 7.6	

PULSE TRAIN OUTPUT DUTY CYCLES:

4.8 KHZ 49%

1.92 KHZ 49.5%

1.6 KHZ 49.5%

D* is Distortion Factor Measured with a H.P. Distortion Analyzer in Conjunction with A TRMS Voltmeter

VISUAL OPERATIONAL TESTS

	28V	25V	30V
Turn on & off into No Load - Repeat several times.	✓	✓	✓
Apply balanced short & remove it into a balanced No Load condition - Repeat several times.	✓	✓	✓
Switch to 150% load, turn inverter on & off several times.	✓	✓	✓
Switch to a balanced short circuit, turn inverter on & off several times (observe input DC current).	✓	✓	✓
Switch to unbalanced overload, two phases open, third shorted, turn on & off several times (observe open phase)	✓	✓	✓
Switch to 100% load, short one phase; remove short.	✓	✓	✓
Switch to 150% load, short one phase; remove short.	✓	✓	✓
Turn on into inductive load-Repeat several times, do same at each of other two input voltages	✓	✓	✓
Connect up continuously varying load & vary it throughout its complete range; repeat several times. Then do same at each of other two input voltages.	✓	✓	✓
Check pulse train outputs for correct frequency & duty cycle	✓	✓	✓

75 VA INVERTER TEST DATA

DATE 12-27-66 UNIT UNDER TEST 1003 DATA BY L. J. B. AMBIENT TEMP. +25°C

VIN \ P_O	(NO LOAD) 0%	(27Ω∆) 100%	(18Ω∆) 150%	(5Ω∆) Overload	Balanced Short Circuit
25 VDC	VAB 26.15 VBC 26.15 VCA 26.15	VAB 26.0 VBC 26.0 VCA 26.0	VAB 25.8 VBC 25.85 VCA 25.85	VAB 7.5 VBC 7.5 VCA 7.5	
28 VDC	VAB 26.15 VBC 26.15 VCA 26.15 Iin .60A η — D* 2.7%	VAB 26.0 VBC 26.0 VCA 26.05 Iin 4.04A η 66.4% D* 3.1%	VAB 25.85 VBC 25.9 VCA 25.9 Iin 6.10A η 65.5% D* 3.8%	VAB 7.5 VBC 7.5 VCA 7.5 Iin 3.21A η 37.6% D* 3.5%	Iin 1.87A
30 VDC	VAB 26.2 VBC 26.0 VCA 26.2	VAB 26.0 VBC 26.05 VCA 26.1	VAB 25.9 VBC 25.95 VCA 25.95	VAB 7.5 VBC 7.55 VCA 7.55	

PULSE TRAIN OUTPUT DUTY CYCLES:

4.8 KHZ 48.5%

1.92 KHZ 49.5%

1.6 KHZ 49.5%

D* is Distortion Factor Measured with a H.P. Distortion Analyzer in Conjunction with A TRMS Voltmeter

VISUAL OPERATIONAL TESTS

	28V	25V	30V
Turn on & off into No Load - Repeat several times.	✓	✓	✓
Apply balanced short & remove it into a balanced No Load condition - Repeat several times.	✓	✓	✓
Switch to 150% load, turn inverter on & off several times.	✓	✓	✓
Switch to a balanced short circuit, turn inverter on & off several times (observe input DC current).	✓	✓	✓
Switch to unbalanced overload, two phases open, third shorted, turn on & off several times (observe open phase)	✓	✓	✓
Switch to 100% load, short one phase; remove short.	✓	✓	✓
Switch to 150% load, short one phase; remove short.	✓	✓	✓
Turn on into inductive load-Repeat several times, do same at each of other two input voltages	✓	✓	✓
Connect up continuously varying load & vary it throughout its complete range; repeat several times. Then do same at each of other two input voltages.	✓	✓	✓
Check pulse train outputs for correct frequency & duty cycle	✓	✓	✓

75 VA INVERTER TEST DATA

DATE 12-27-66 UNIT UNDER TEST 1003 DATA BY L.J.B. AMBIENT TEMP. 50°C

P_O / VIN	(NO LOAD) 0%	(27ΩΔ) 100%	(18ΩΔ) 150%	(5ΩΔ) Overload	Balanced Short Circuit
25 VDC	VAB 26.0 VBC 26.0 VCA 26.0	VAB 25.9 VBC 25.95 VCA 25.95	VAB 25.6 VBC 25.7 VCA 25.7	VAB 7.5 VBC 7.55 VCA 7.55	
28 VDC	VAB 26.0 VBC 26.05 VCA 26.05 Iin .60A η — D*	VAB 25.9 VBC 25.95 VCA 25.95 Iin 4.07A η 65.6% D*	VAB 25.65 VBC 25.7 VCA 25.7 Iin 6.17A η 63.6% D*	VAB 7.5 VBC 7.55 VCA 7.55 Iin 3.33A η 36.6% D*	Iin 1.93A
30 VDC	VAB 26.0 VBC 26.05 VCA 26.05	VAB 26.0 VBC 26.0 VCA 26.0	VAB 25.7 VBC 25.75 VCA 25.75	VAB 7.5 VBC 7.55 VCA 7.55	

PULSE TRAIN OUTPUT DUTY CYCLES:

4.8 KHZ 48%

1.92 KHZ 49%

1.6 KHZ 49%

D* is Distortion Factor Measured with a H.P. Distortion Analyzer in Conjunction with A TRMS Voltmeter

VISUAL OPERATIONAL TESTS

	28V	25V	30V
Turn on & off into No Load - Repeat several times.	✓	✓	✓
Apply balanced short & remove it into a balanced No Load condition - Repeat several times.	✓	✓	✓
Switch to 150% load, turn inverter on & off several times.	✓	✓	✓
Switch to a balanced short circuit, turn inverter on & off several times (observe input DC current).	✓	✓	✓
Switch to unbalanced overload, two phases open, third shorted, turn on & off several times (observe open phase)	✓	✓	✓
Switch to 100% load, short one phase; remove short.	✓	✓	✓
Switch to 150% load, short one phase; remove short.	✓	✓	✓
Turn on into inductive load-Repeat several times, do same at each of other two input voltages	✓	✓	✓
Connect up continuously varying load & vary it throughout its complete range; repeat several times. Then do same at each of other two input voltages.	✓	✓	✓
Check pulse train outputs for correct frequency & duty cycle	✓	✓	✓

T1-2908

DATA SHEET (16-25)

TAKEN BY	DATE	PAGE OF
L. J. B.	12-27-66	1

% FULL LOAD VS. % DISTORTION

28 VDC INPUT UNIT # 1003

% FULL LOAD	LOAD RES.	% DIST.
0	∞ Ω	2.83
10	270	2.98
18	150	2.97
27	100	2.96
50	54	2.85
100	27	3.10
150	18	3.72
133	16	3.73
115	14	3.69
84	10	3.51
42	5	3.46

T1-2908

DATA SHEET (16-25)

TAKEN BY	DATE	PAGE OF
L. J. B.	12-27-66	1

DATA ON OUTPUT VOLTAGE AND CURRENT CHARACTERISTIC

28 VDC INPUT UNIT # 1003

V_{OUT}		I_{OUT}
26.1V		.106A
26.1		.189
26.1		.30
26.1		.77
26.1		1.50
26.0		1.90
26.0		2.15
25.4		2.52
23.8		2.53
19.0		2.56
7.5		2.50
3φ SHORT		2.45

75 VA INVERTER TEST DATA

DATE 1-26-67 UNIT UNDER TEST 1004 DATA BY L.J.B. AMBIENT TEMP. -25°C

VIN \ PO	(NO LOAD) 0%	(27Ω) 100%	(18Ω) 150%	(5Ω) Overload	Balanced Short Circuit
25 VDC	VAB 26.35 VBC 26.35 VCA 26.35	VAB 26.2 VBC 26.2 VCA 26.15	VAB 26.05 VBC 26.05 VCA 26.0	VAB 7.6 VBC 7.6 VCA 7.6	
28 VDC	VAB 26.35 VBC 26.35 VCA 26.35 Iin .61A n — D*	VAB 26.3 VBC 26.3 VCA 26.3 Iin 4.07A n 67.9% D*	VAB 26.15 VBC 26.15 VCA 26.1 Iin 6.03A n 67.5% D*	VAB 7.6 VBC 7.6 VCA 7.6 Iin 3.13A n 39.6% D*	Iin 1.78A
30 VDC	VAB 26.4 VBC 26.4 VCA 26.4	VAB 26.35 VBC 26.35 VCA 26.35	VAB 26.2 VBC 26.2 VCA 26.15	VAB 7.6 VBC 7.6 VCA 7.6	

PULSE TRAIN OUTPUT DUTY CYCLES:

4.8 KHZ 49%

1.92 KHZ 49.5%

1.6 KHZ 50%

D* is Distortion Factor Measured with a H.P. Distortion Analyzer in Conjunction with A TRMS Voltmeter

VISUAL OPERATIONAL TESTS

Test	28V	25V	30V
Turn on & off into No Load - Repeat several times.	✓	✓	✓
Apply balanced short & remove it into a balanced No Load condition - Repeat several times.	✓	✓	✓
Switch to 150% load, turn inverter on & off several times.	✓	✓	✓
Switch to a balanced short circuit, turn inverter on & off several times (observe input DC current).	✓	✓	✓
Switch to unbalanced overload, two phases open, third shorted, turn on & off several times (observe open phase)	✓	✓	✓
Switch to 100% load, short one phase; remove short.	✓	✓	✓
Switch to 150% load, short one phase; remove short.	✓	✓	✓
Turn on into inductive load-Repeat several times, do same at each of other two input voltages	✓	✓	✓
Connect up continuously varying load & vary it throughout its complete range; repeat several times. Then do same at each of other two input voltages.	✓	✓	✓
Check pulse train outputs for correct frequency & duty cycle	✓	✓	✓

75 VA INVERTER TEST DATA

DATE 1-26-67 UNIT UNDER TEST 1004 DATA BY L.J.B. AMBIENT TEMP. +25°C

R_O / VIN	(NO LOAD) 0%	(27Ω∆) 100%	(18Ω∆) 150%	(5Ω∆) Overload	Balanced Short Circuit
25 VDC	VAB 26.05 VBC 26.05 VCA 26.05	VAB 26.0 VBC 26.0 VCA 26.0	VAB 25.8 VBC 25.8 VCA 25.8	VAB 7.55 VBC 7.5 VCA 7.5	
28 VDC	VAB 26.05 VBC 26.05 VCA 26.05 Iin .60A η — D*	VAB 26.0 VBC 26.0 VCA 26.0 Iin 3.98A η 67.4% D*	VAB 25.9 VBC 25.85 VCA 25.85 Iin 6.02A η 66.0% D*	VAB 7.55 VBC 7.5 VCA 7.5 Iin 3.20A η 36.7% D*	Iin 1.87A
30 VDC	VAB 26.1 VBC 26.1 VCA 26.1	VAB 26.05 VBC 26.05 VCA 26.05	VAB 25.9 VBC 25.9 VCA 25.9	VAB 7.55 VBC 7.5 VCA 7.5	

PULSE TRAIN OUTPUT DUTY CYCLES:

4.8 KHZ 48%

1.92 KHZ 49%

1.6 KHZ 50%

D* is Distortion Factor Measured with a H.P. Distortion Analyzer in Conjunction with A TRMS Voltmeter

VISUAL OPERATIONAL TESTS

	28V	25V	30V
Turn on & off into No Load - Repeat several times.	✓	✓	✓
Apply balanced short & remove it into a balanced No Load condition - Repeat several times.	✓	✓	✓
Switch to 150% load, turn inverter on & off several times.	✓	✓	✓
Switch to a balanced short circuit, turn inverter on & off several times (observe input DC current).	✓	✓	✓
Switch to unbalanced overload, two phases open, third shorted, turn on & off several times (observe open phase)	✓	✓	✓
Switch to 100% load, short one phase; remove short.	✓	✓	✓
Switch to 150% load, short one phase; remove short.	✓	✓	✓
Turn on into inductive load-Repeat several times, do same at each of other two input voltages	✓	✓	✓
Connect up continuously varying load & vary it throughout its complete range; repeat several times. Then do same at each of other two input voltages.	✓	✓	✓
Check pulse train outputs for correct frequency & duty cycle	✓	✓	✓

75 VA INVERTER TEST DATA

DATE 1-26-67 UNIT UNDER TEST 1004 DATA BY L. J. B. AMBIENT TEMP. 50°C

R_O \ VIN	(NO LOAD) 0%	(27Ω∆) 100%	(18Ω∆) 150%	(5Ω∆) Overload	Balanced Short Circuit
25 VDC	VAB 26.0 VBC 26.05 VCA 26.05	VAB 26.0 VBC 25.95 VCA 25.95	VAB 25.8 VBC 25.8 VCA 25.8	VAB 7.5 VBC 7.5 VCA 7.5	
28 VDC	VAB 26.05 VBC 26.05 VCA 26.05 Iin .60A η — D*	VAB 26.0 VBC 26.0 VCA 26.0 Iin 4.00A η 67.1% D*	VAB 25.8 VBC 25.8 VCA 25.8 Iin 6.10A η 64.9% D*	VAB 7.5 VBC 7.5 VCA 7.5 Iin 3.25A η 37.0% D*	Iin 1.90A
30 VDC	VAB 26.1 VBC 26.1 VCA 26.1	VAB 26.0 VBC 26.0 VCA 26.0	VAB 25.8 VBC 25.8 VCA 25.8	VAB 7.5 VBC 7.5 VCA 7.5	

PULSE TRAIN OUTPUT DUTY CYCLES:

4.8 KHZ 47%

1.92 KHZ 49.5%

1.6 KHZ 50%

D* is Distortion Factor Measured with a H.P. Distortion Analyzer in Conjunction with A TRMS Voltmeter

VISUAL OPERATIONAL TESTS

	28V	25V	30V
Turn on & off into No Load - Repeat several times.	✓	✓	✓
Apply balanced short & remove it into a balanced No Load condition - Repeat several times.	✓	✓	✓
Switch to 150% load, turn inverter on & off several times.	✓	✓	✓
Switch to a balanced short circuit, turn inverter on & off several times (observe input DC current).	✓	✓	✓
Switch to unbalanced overload, two phases open, third shorted, turn on & off several times (observe open phase)	✓	✓	✓
Switch to 100% load, short one phase; remove short.	✓	✓	✓
Switch to 150% load, short one phase; remove short.	✓	✓	✓
Turn on into inductive load-Repeat several times, do same at each of other two input voltages	✓	✓	✓
Connect up continuously varying load & vary it throughout its complete range; repeat several times. Then do same at each of other two input voltages.	✓	✓	✓
Check pulse train outputs for correct frequency & duty cycle	✓	✓	✓

APPENDIX D

FREQUENCY DEVIATION VERSUS TEMPERATURE

THE Bendix CORPORATION

PIONEER-CENTRAL DIVISION

DAVENPORT, IOWA

PRESENTS

AN ENGINEERING PROPOSAL

FOR A TEMPERATURE

COMPENSATED CRYSTAL OSCILLATOR

TO

TEXAS INSTRUMENTS INC.

DALLAS, TEXAS

ELECTRONICS SECTION

Prepared by
THE BENDIX CORPORATION
PIONEER-CENTRAL DIVISION
Davenport, Iowa

AN ENGINEERING PROPOSAL
FOR A TEMPERATURE
COMPENSATED CRYSTAL OSCILLATOR

Prepared for

TEXAS INSTRUMENTS INC.
Dallas, Texas

Pub. No. 1-52012 (3370-65)
June 16, 1965

PROPRIETARY RIGHTS

DURATION OF OFFER

This proposal, type numbers assigned, and drawings and data contained herein shall be considered null and void after December 16, 1965, unless contractually accepted or said date extended in writing by the Pioneer-Central Division of The Bendix Corporation.

THE BENDIX CORPORATION
PIONEER-CENTRAL DIVISION

The Pioneer-Central Division of The Bendix Corporation has for several years been performing research and development in the field of stable frequency generation and its control in extreme environments.

As a result of this work, the Pioneer-Central Division has developed circuit techniques for temperature compensating crystal oscillators, thus eliminating the necessity of precisely controlling the oscillators and/or the crystal environment. The method most frequently used for controlling the temperature environment of the oscillator and/or crystal is to place them in a thermostatically-controlled oven. These ovens generally consume considerable power, generate RF interference, and require a long stabilization time as well as being relatively large in size and weight. Though adequate in many instances, ovens are not well suited for applications where size, weight, power consumption, and instantaneous operation without warm-up are important design considerations.

The temperature compensation method developed at Pioneer-Central employs a technique by which circuit elements are temperature sensitive; that is, their nominal values vary as some function of temperature. By proper utilization of the temperature characteristics of these passive elements and careful consideration of the active elements of the oscillator circuit, it is possible to produce oscillators which exhibit excellent frequency stability versus temperature.

The detailed selection of temperature sensitive elements is not required since computer programs have been developed which generate the specific values for the elements for any given oscillator design. This has resulted in Pioneer-Central being able to mass produce temperature compensated crystal oscillators.

As a result of this activity in the manufacture of ovenless frequency standards, Bendix Pioneer-Central is pleased to propose to Texas Instruments, Incorporated a temperature compensated crystal oscillator using integrated circuits with the following specifications.

Output Frequency: 2.4576 MC

Frequency Stability:

Short Term: 1×10^{-7} for a quarter-second period at a constant temperature.

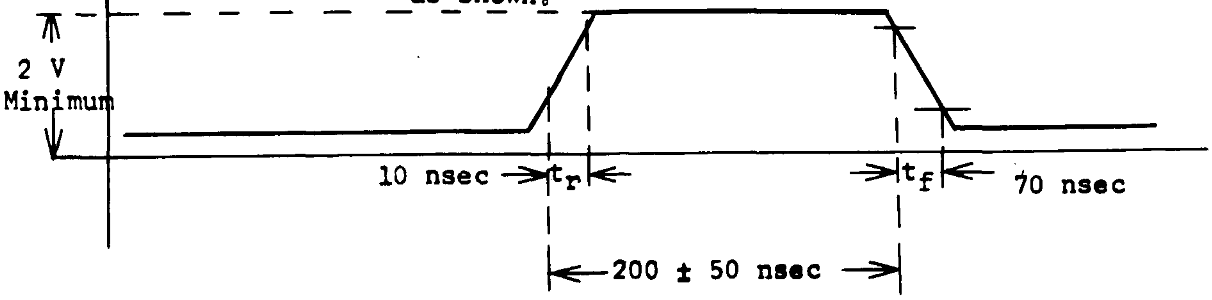
Long Term: 2 ppm/year with a 1 ppm/year design goal.

Over Temperature: ± 15 ppm -25°C to +110°C and ± 25 ppm +110°C to +125°C. Maximum rate of change of temperature 1°C per minute.

Input Power: 150 mw @ 12 V DC guaranteed, design goal of 50 mw with proper supplies. See technical discussion.

Reliability Prediction: Better than 0.999 per 100 hours of operation based on Parts Count Analysis per MIL-HDBK-217.

Output Waveform: Two volt peak-to-peak minimum pulse into 2 K ohm load as shown.



Physical Parameters: 1" x 1" x 1" guaranteed with a design goal of 0.5 cubic inches. Printed circuit mounting using solder lugs (wire mounting furnished if specified)

Environmental Specifications: The oscillator will be designed to meet the following specifications.

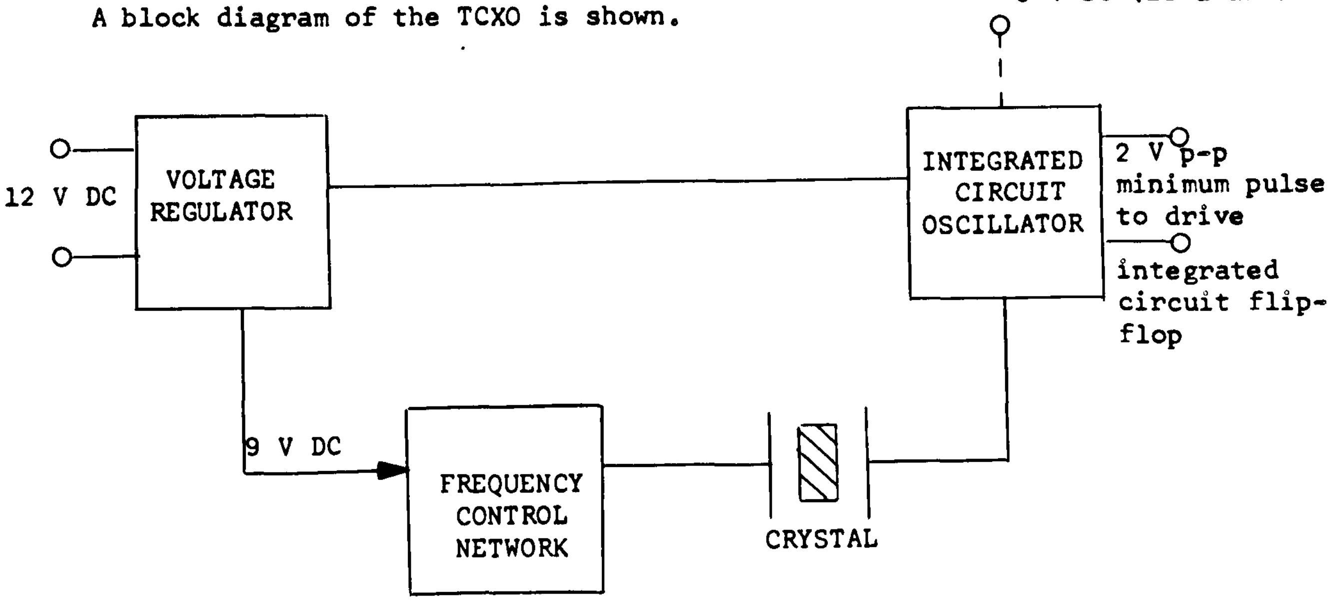
(1) Temperature cycling -55°C to +200°C, 5 cycles (nonoperation).
(2) Moisture resistance per MIL-STD-202 (10) cycles.
(3) A design goal of 100 g acceleration for 5 minutes.
(4) Storage at +200°C for 1000 hours.

The oscillator will be tested to the following specifications.

(1) Vibration 20 g, 0 to 2000 cps, three 17 minute sweeps per axis.
(2) Shock 50 g, 10 millisecond pulse with a design goal of 150 g, 10 ms.

The performance of the oscillator cannot be guaranteed under a radiation environment, since test facilities and radiation test data are not available. Every effort will be made, however, to design a unit which will operate to specification under adverse environmental conditions such as radiation exposure.

A block diagram of the TCXO is shown.



A voltage regulator composed of a discrete resistor and zener diode is used to eliminate B+ voltage variations. The regulated supply is required for the frequency control network to achieve the necessary frequency stability. If a 12 V DC supply with 1% or better regulation is furnished, the regulator could be omitted. In addition, if a 6 V DC supply could be furnished, total power consumption could be further reduced.

The basic oscillator is composed of an integrated circuit amplifier, a quartz crystal, and a frequency control network. The crystal cannot be integrated and the thermistors in the control network make integration of this portion difficult.

The oscillator output, taken directly from the integrated circuit, is shown in the specification section of this proposal.

The temperature compensated crystal oscillators developed by Pioneer-Central are being used in various applications such as computer clocks, inverter frequency control and master oscillators for satellite communication systems. In addition to this, Pioneer-Central is performing basic research in temperature compensation techniques for the U. S. Army Electronics Laboratories. A partial listing of contracts appears at the end of this proposal.

RELATED EXPERIENCE

The temperature compensated crystal oscillators developed by Pioneer-Central are being used in various applications such as computer clocks, inverter frequency control, and master oscillators for satellite communication systems. In addition to this Pioneer-Central is performing basic research in temperature compensation techniques for the U. S. Army Electronics Laboratories. A partial listing of contracts which have resulted in invaluable knowledge and experience is given below.

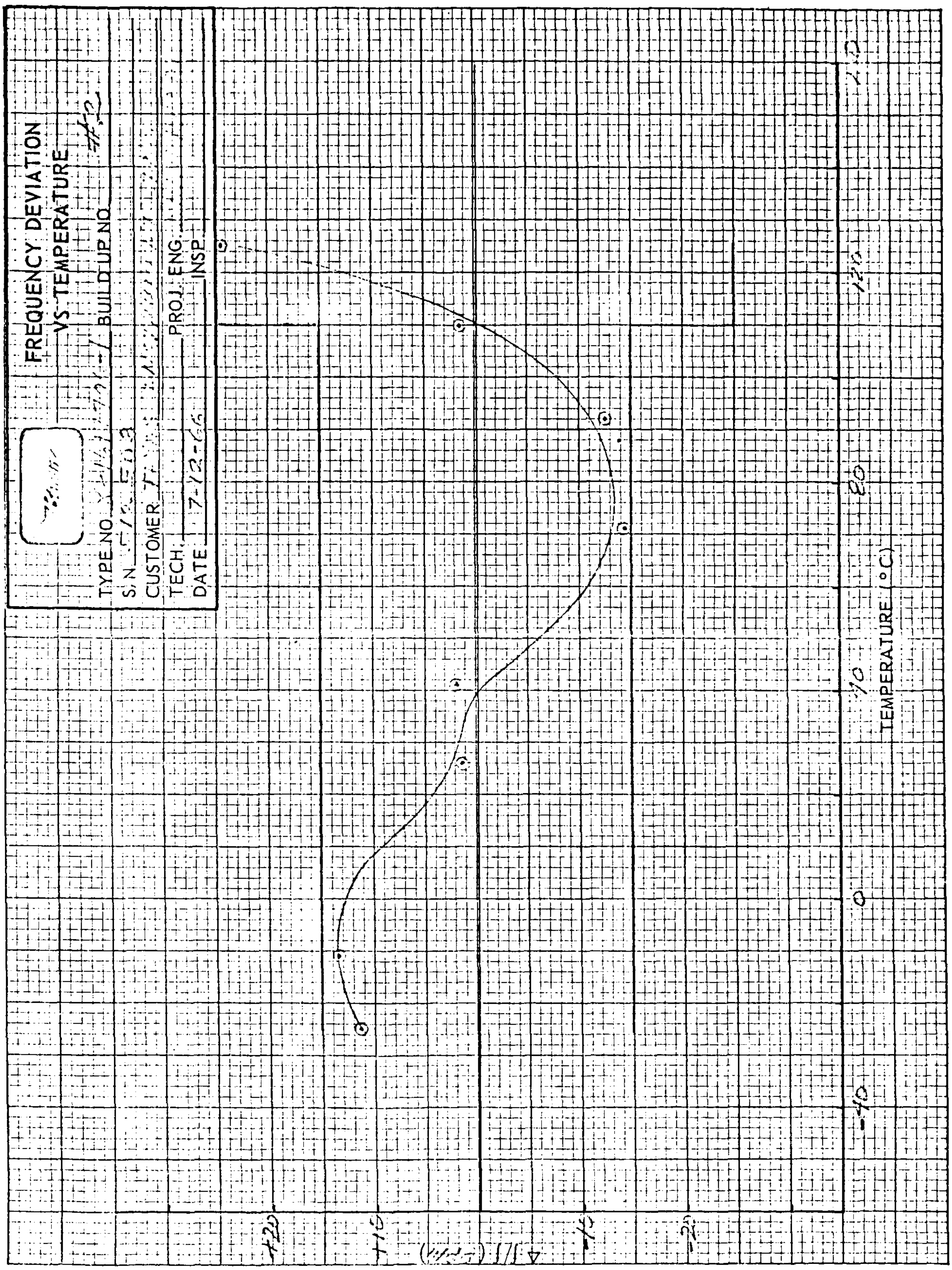
LIST OF PREVIOUS CONTRACTS

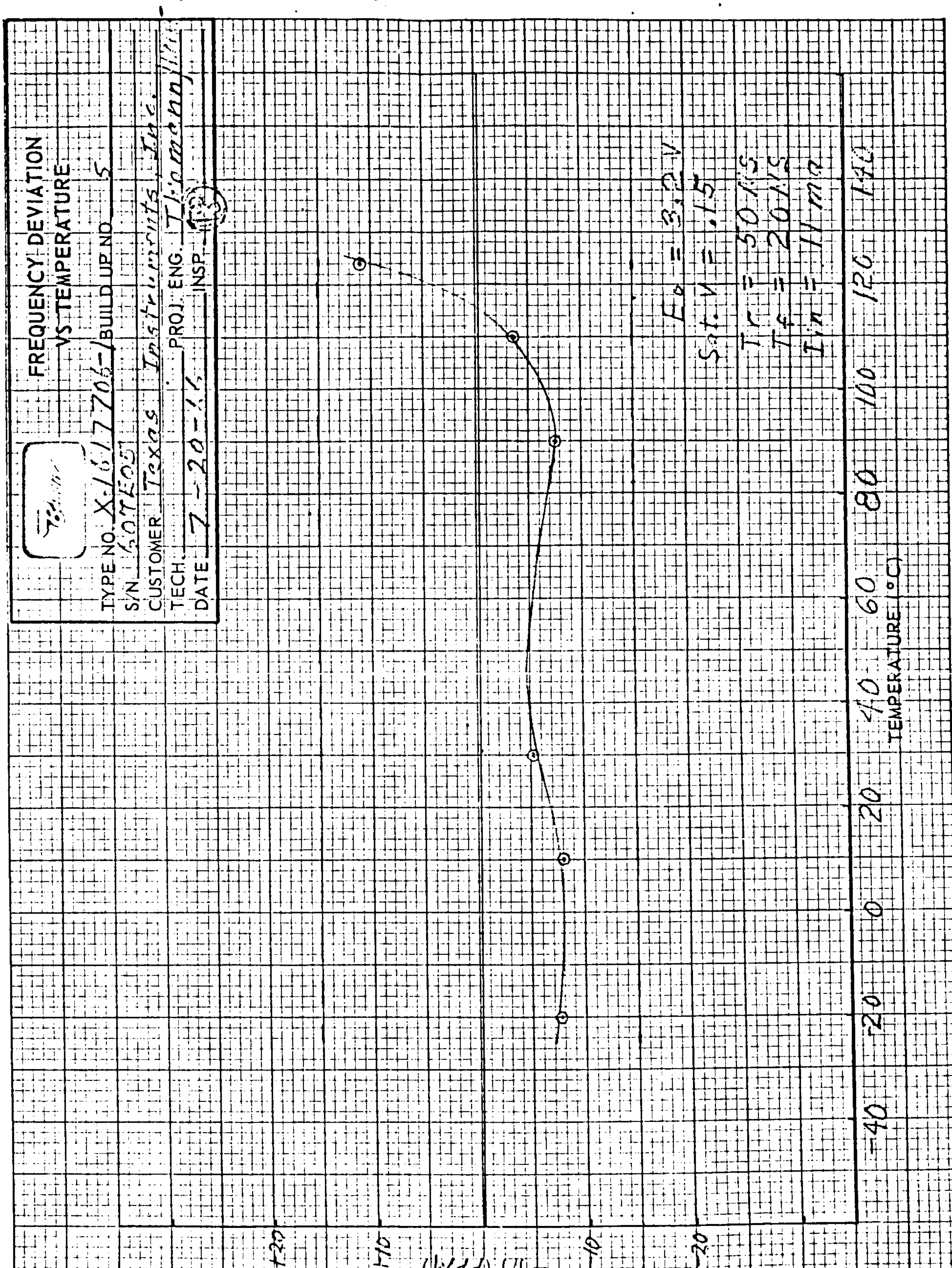
Program Name	Sponsoring Agency	Contract Number	Program Description
Compensated Oscillators for Saturn Research	NASA-MSFC	NAS 8-4779	Output frequencies of 1.2 and 4.8 KC with a stability of 10 ppm over the temperature range of -25°C to +125°C.
Oscillator Compensation Studies	U. S. Army Electronics Laboratories	DA-36-039 SC-90782	Research study on frequency temperature compensation techniques for quartz crystal oscillators.
Quartz Crystal Studies	U. S. Army Electronics Laboratories (McCoy Electronics)	DA-36-039 SC-90802	Research study on temperature compensation of 30 MC, 3rd overtone, quartz crystals.
Oscillator Development	U. S. Army Electronics Laboratories	DA-28-043 AMC-00042(E)	Systematic development of quartz crystal oscillators for integration in portable SSB radio sets.
960 KC Frequency Standard for Advanced Minuteman	North American Autonetics	Z-34B811399	Square wave output, stable to 1 ppm over the temperature range of 15°C to 27°C and 5 ppm in 3 years.
50 MC Phase Locked Oscillator for ADVENT	Bendix Systems Division		Sine wave output, stable to 1 ppm over temperature range -40 to +70°C.

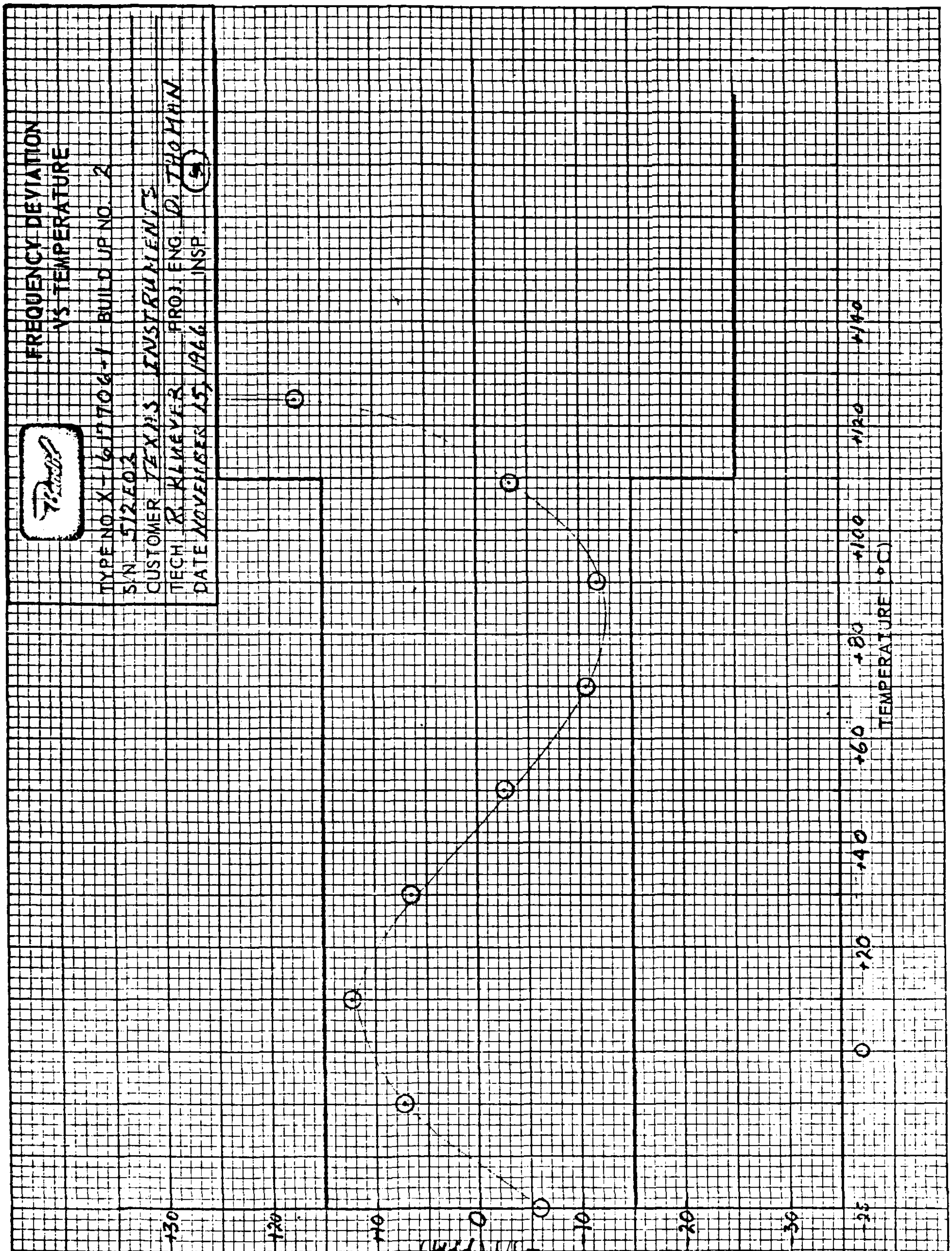
Program Name	Sponsoring Agency	Contract Number	Program Description
1 and 5 MC Frequency Standard for Back-Pack Radio	Avco	E-54058	Reference signal output stable to 0.25 ppm over -40 to +70°C.
3.2 MC Master Oscillator for Nimbus Satellite	California Computer	1578-107	Stable to 0.1 ppm ~~from 0~~ to 50°C.
4 KC, Time Base for Sergeant Launcher	Sperry-Utah	9871	Stable to 10 ppm from -40 to +65°C.
1 and 8 MC TCXO for Sergeant Computer	Sperry-Utah	121273	Square wave -8 V p-p 10 ppm for -40 to 125°C.
2.048 MC Frequency Standard for LAENS Navigational System	A-C Spark Plug	ENP-65094	Stable to 0.5 ppm from 0 to 70°C and 5 ppm from -55 to 0°C.
400 Cycle Inverter Frequency Control	Bendix Red Bank	RB 339530	Frequency standard for static inverter. Stable to 15 ppm over -40 to 125°C.
14 MC TCXO for Atomichron	National Company	S-45411	Voltage controlled temperature compensated frequency standard. Stable to 0.1 ppm over 0 to +50°C.
2.048 MC Clock	Magnavox Co.	WW22446-6JA	Stable to 0.03 ppm over -10 to +50°C.
115 MC Frequency Standard	Magnavox Co.	WW21433RT	Stable to 5 ppm over -40 to +60°C.
300 KC TCXO for Sidewinder Radar Timing	NOTS, China Lake, California	60530/3640Y9824-63	Voltage controlled temperature compensated frequency standard. Stable to 10 ppm over -60 to +105°C.
Dual 4.8 KC & 1.2 KC TCXO for Saturn Research	NASA-MSFC	NAS 8-5462	Redundant oscillators plus a multivibrator for reliability over -25 to +125°C.

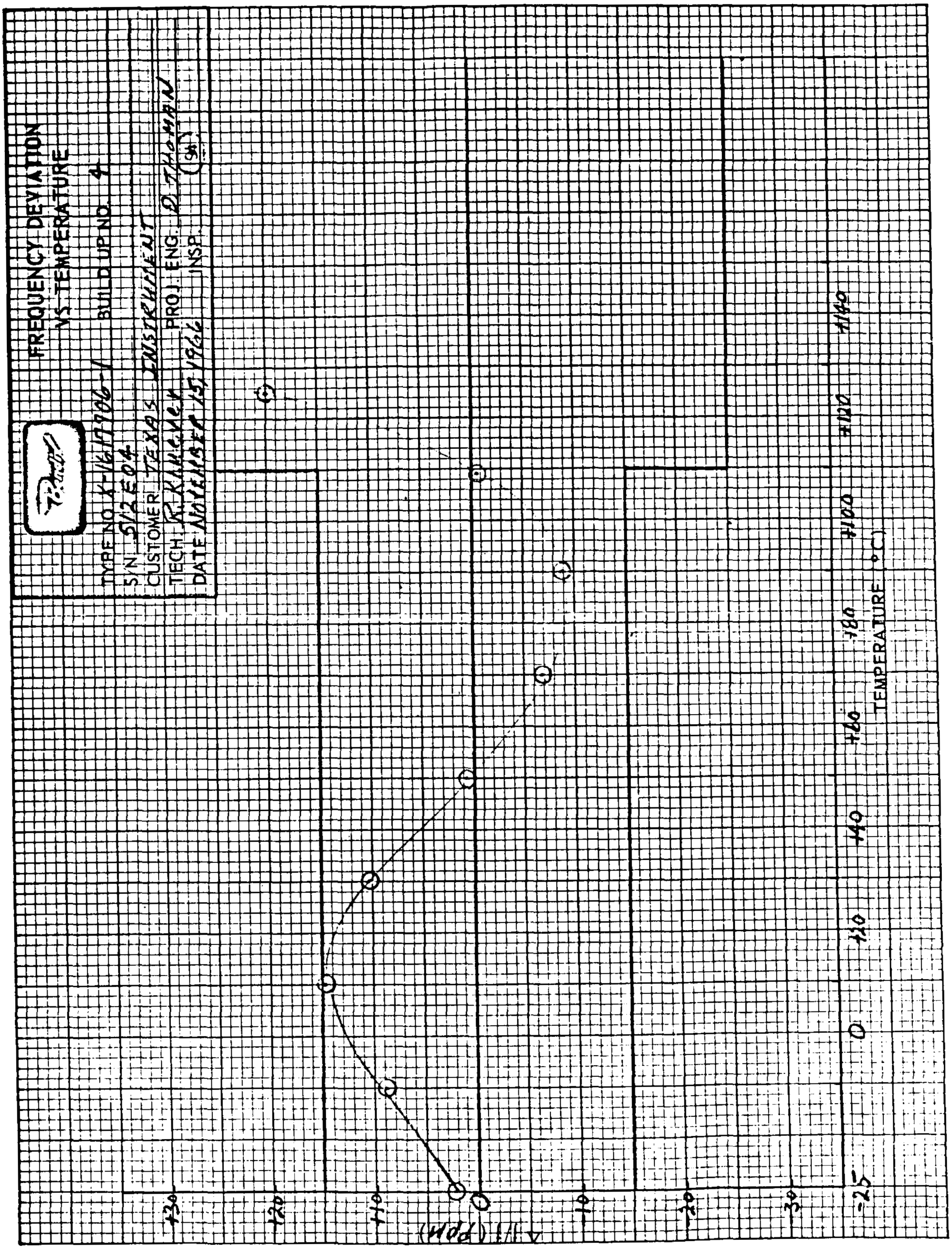
Program Name	Sponsoring Agency	Contract Number	Program Description
Central Timing Oscillator for Apollo Project	NAA	NAS 9-150 #M4J3XA-705511	Oscillator switches "on" automatically on loss of input signal. Stable to 2 ppm over -10 to +50°C.
19.2 KC TCXO for Saturn Stable Platform	Bendix Eclipse-Pioneer	NAS 8-1577 54-061487	Stable to 10 ppm over -30 to +100°C.
90.902 MC, 106.80 MC TCXO for Communications Satellite	M.I.T. Lincoln Labs	CC-607	Maintains a difference frequency stable to 0.03 ppm over -20 to +50°C when multiplied to X-band frequency.
100 KC TCXO for Phoenix Weapons Systems	A. W. Haydon Company	35878	Stable to 1 ppm over -40 to +70°C.
3.2 KC TCXO for Pershing Inverter Control	Westinghouse Electric Corp., Lima, Ohio	39-F.372680	Stable to 30 ppm over -32 to +100°C.
4 MC Aircraft Timing Oscillator	Litton	W-683181	Stable to 50 ppm over -55 to +123°C.
614.4 KC Frequency Standard	Boeing Company Seattle	N-651340-6892	Stable to 1 ppm over +5 to +65°C.
1 MC TCXO	Stanford Research Institute	B-58826-U5	Stable to 0.1 ppm over -10 to +50°C and to 1 ppm over -40 to +60°C.
113.05 MC TCXO for Communications Satellite	M.I.T. Lincoln Labs	AA 3133	Stable to 1 ppm over -20 to +50°C.
118.5 MC TCXO for Communications Satellite	M.I.T. Lincoln Labs	AA 3134	Stable to 1 ppm over -20 to +50°C.

Program Name	Sponsoring Agency	Program Description
2.3040 MC & 72 KC ISIS Satellite Oscillator	Defense Research Board, Canada	Stable to 0.1 ppm over -40 to +70°C.
1 KC X-15 Aircraft Timing Oscillator	NASA, Edwards AFB	Stable to 10 ppm over -30 to +85° C.
Various frequencies from 5 to 86 MC for NASA radar projects	ITT, Federal Labs California	Stable to 1 ppm over -10 to +60°C.
21 MC TCXO for ADIA Radar	Westinghouse Electric Corp., Baltimore, Md.	Stable to 1 ppm over -20 to 90°C, to 2.5 ppm over 90 to 100°C, and 7.5 ppm over 100 to 110°C.
5 MC TCXO for Back-Pack Radio	Telefunken AC, Germany Plessey Company	Stable to 1 ppm over -40 to +70°C at 60 MW maximum input power.
31.84 MC Voltage Controlled TCXO for Space Tracking Radar	Jet Propulsion Laboratories	Stable to 1 ppm over 15°C to 35°C. Control of 100 cps/volt for ± 10 voltage range.


FREQUENCY DEVIATION
VS TEMPERATURE
TYPE NO.
BUILD UP NO.
S/N
CUSTOMER
TECH.
PROJ. ENG.
DATE
7-12-66
INSP.
TEMPERATURE (°C)


FREQUENCY DEVIATION
VS TEMPERATURE
BUILD UP NO. 5
TYPE NO. X-1617706-1
S/N 607E05
CUSTOMER Texas Instruments, Inc.
TECH.
PROJ. ENG.
DATE 7-20-66
INSP.
Eo = 3.2 V
Sat. V = .15
Tr = 50 ns
Tf = 20 ns
Iin = 11 ma
-40 -20 0 20 40 60 80 100 120 140
TEMPERATURE (°C)
+20 +10 -10 -20
Δf/f (PPM)


FREQUENCY DEVIATION
VS TEMPERATURE
TYPE NO
BUILD UP NO. 2
S/N
CUSTOMER TEXAS INSTRUMENTS
TECH
PROJ. ENG. D. THOMAN
DATE NOVEMBER 15, 1966
INSP.
TEMPERATURE °C
+20
+40
+60
+80
+100
+120
+140
+30
+20
+10
0
-10
-20
-30
(PPM)


FREQUENCY DEVIATION
VS TEMPERATURE
BUILD UP NO. 4
TYPE NO
S/N
CUSTOMER
TECH
PROJ ENG
DATE
INSP
TEMPERATURE °C
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+10
0
-10
-20
-30

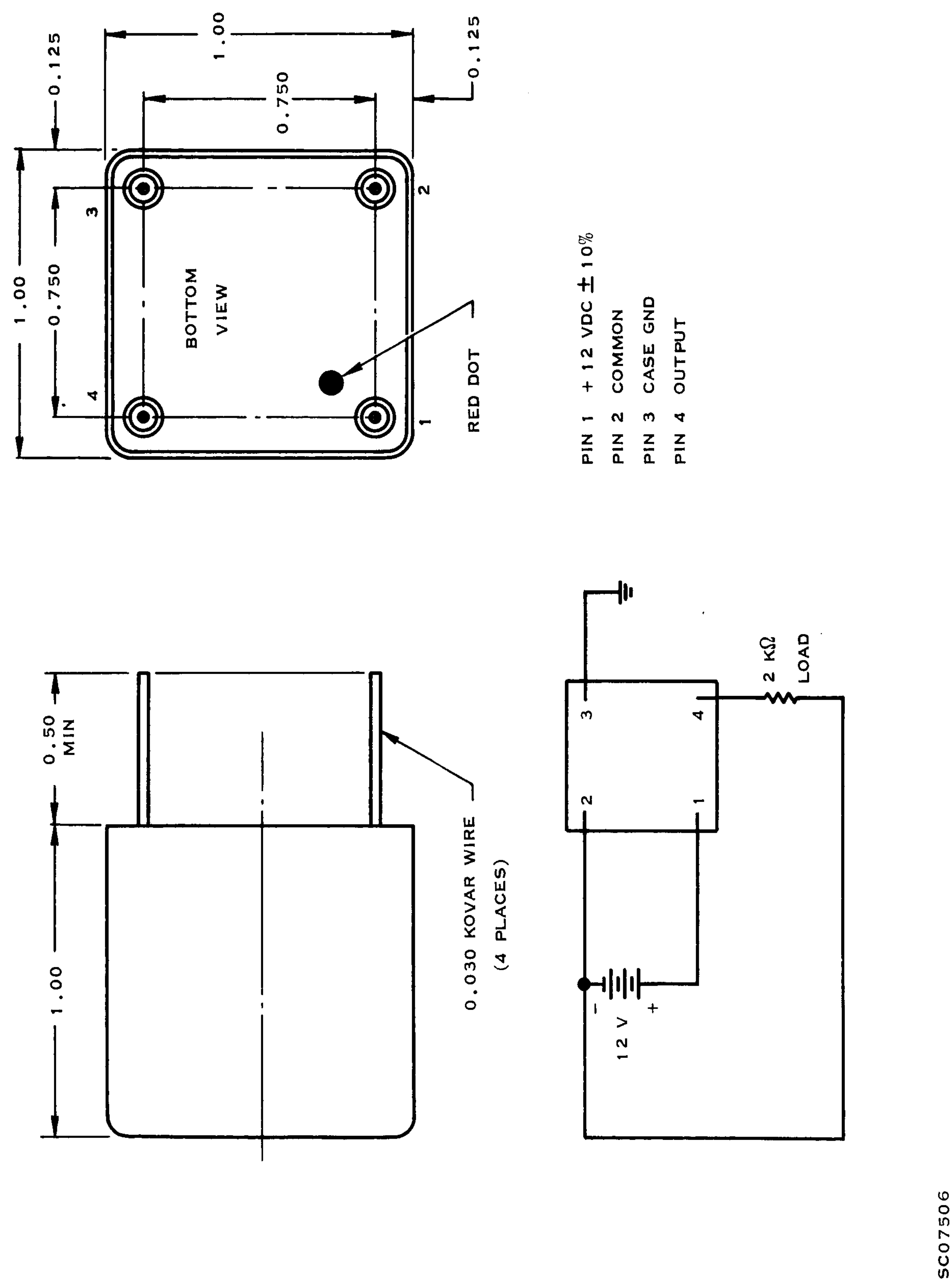
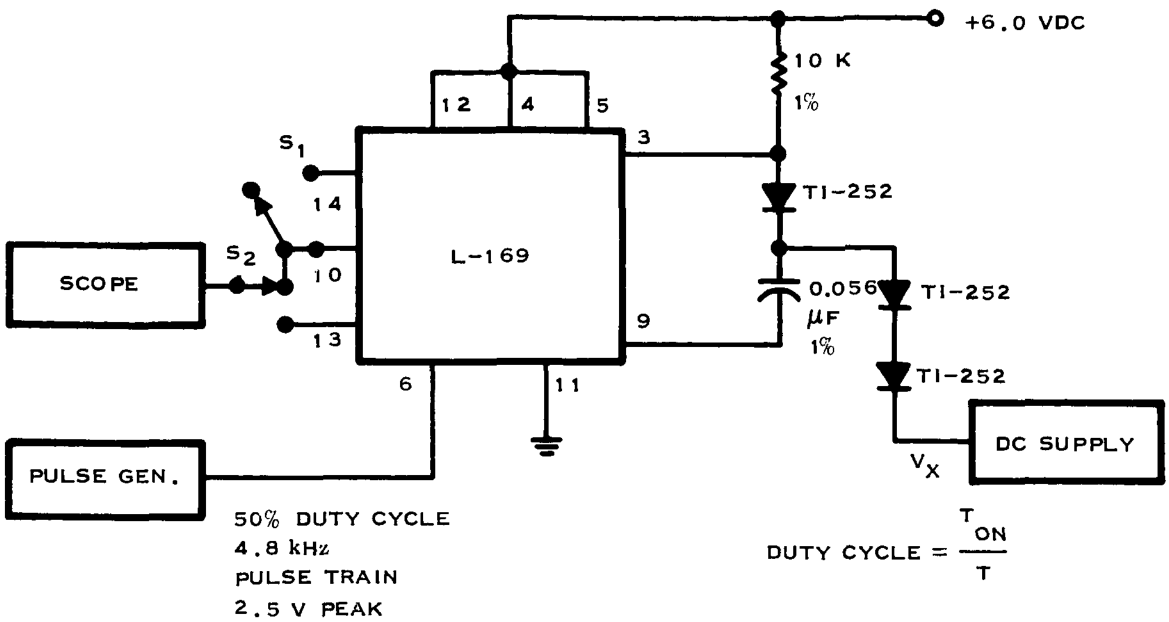


Figure D-5. Texas Instruments 2.4576 MHz TCXO (Outline)

APPENDIX E

ELECTRICAL SPECIFICATIONS FOR L-169

EVALUATION TEST SETUP



TEST "A"

$T_{AMBIENT} = 25^{\circ}C$

S_2 CONNECTED TO PIN 10

S_1 OPEN

V_X ADJUSTED TO GIVE 50% DUTY CYCLE, 4.8 kHz OUTPUT PULSE TRAIN

RESULT: $V_X = 2.6 \pm 0.1$ V

TEST "B"

$T_{AMBIENT} = 25^{\circ}C$

S_2 CONNECTED TO PIN 10

S_1 OPEN

V_X APPLIED

RESULT: DUTY CYCLE OF 4.8 kHz OUTPUT PULSE TRAIN VARIES AS A FUNCTION OF V_X, FOR ALL VALUES OF V_X FROM +0.95 V TO A HIGHER VALUE WHICH CAUSES A 100% DUTY CYCLE.

TEST "C"

REPEAT TEST "B" AT $-25^{\circ}C$ AND $+125^{\circ}C$; RESULTS SHOULD BE IDENTICAL

TEST "D"

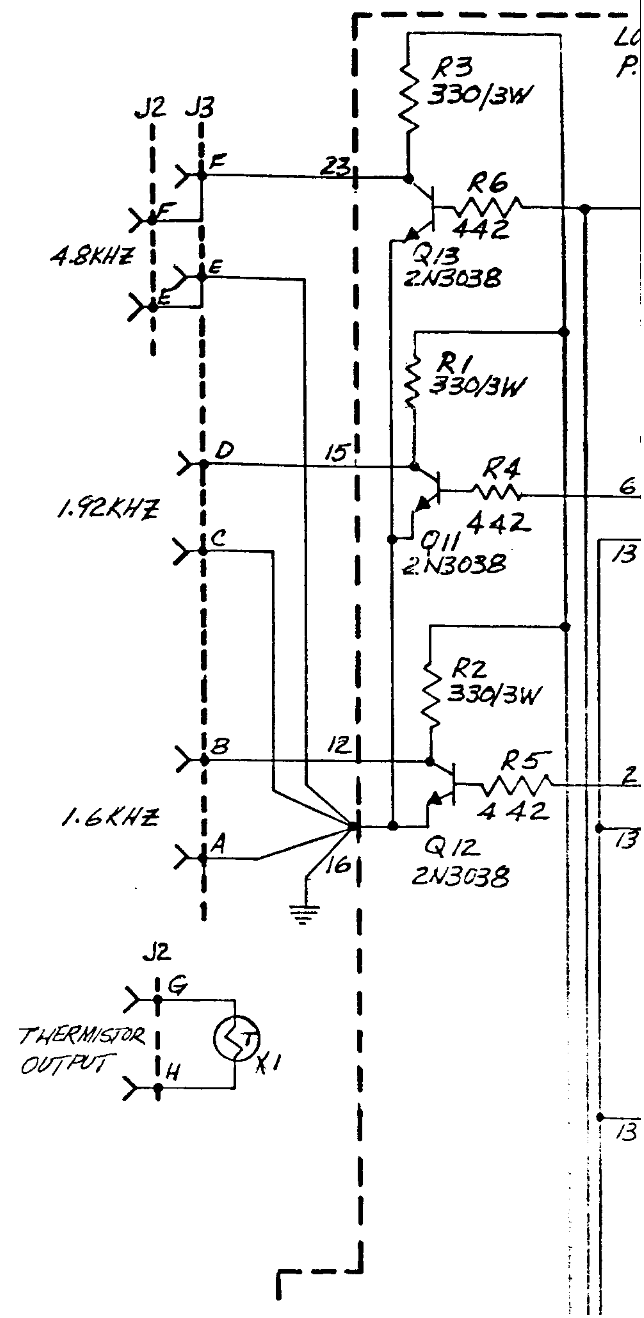
REPEAT TESTS "B" AND "C" WITH S_2 ON PIN 13 AND S_1 CONNECTED TO PIN 14. RESULTS SHOULD BE IDENTICAL.

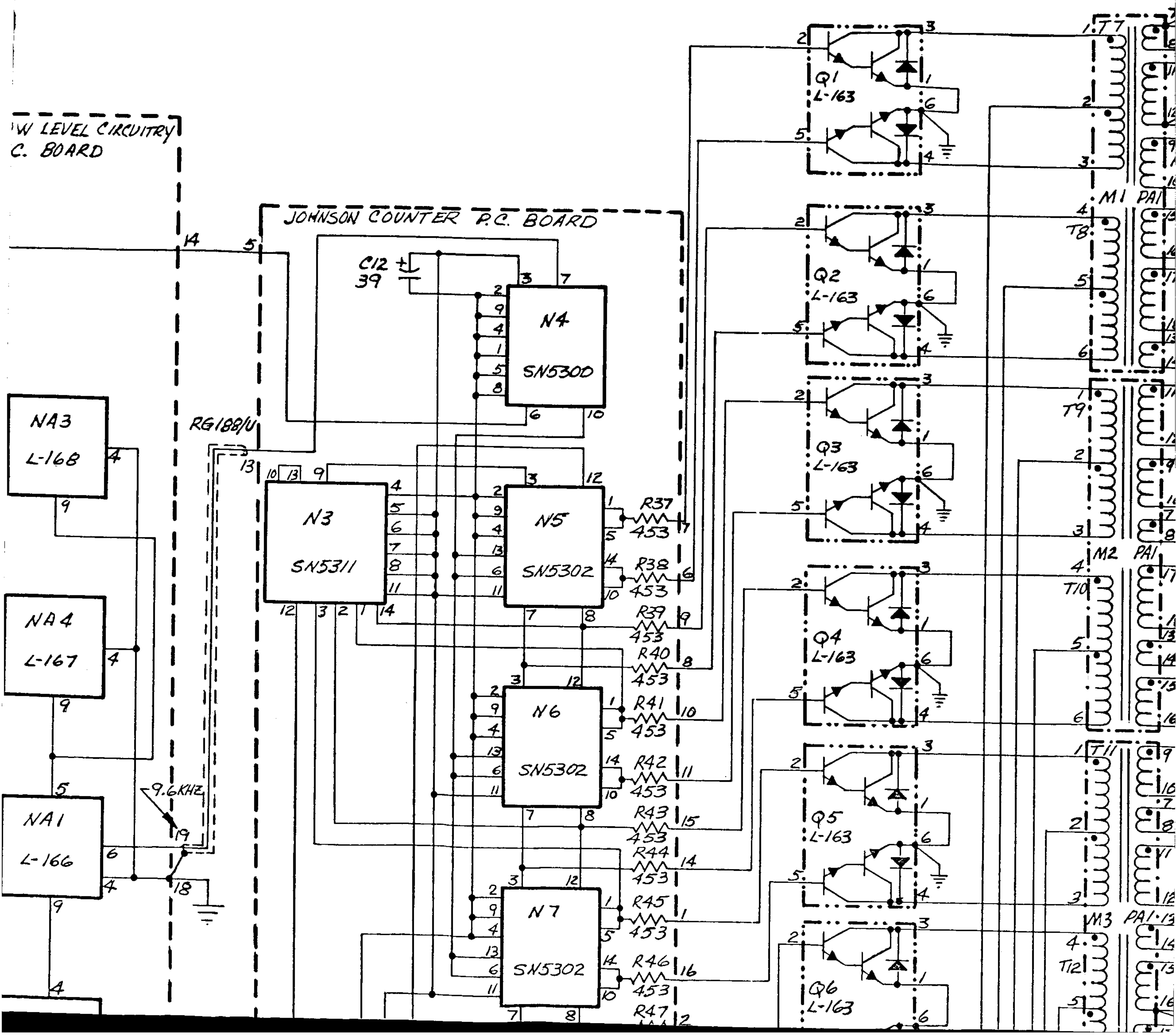
SC07546

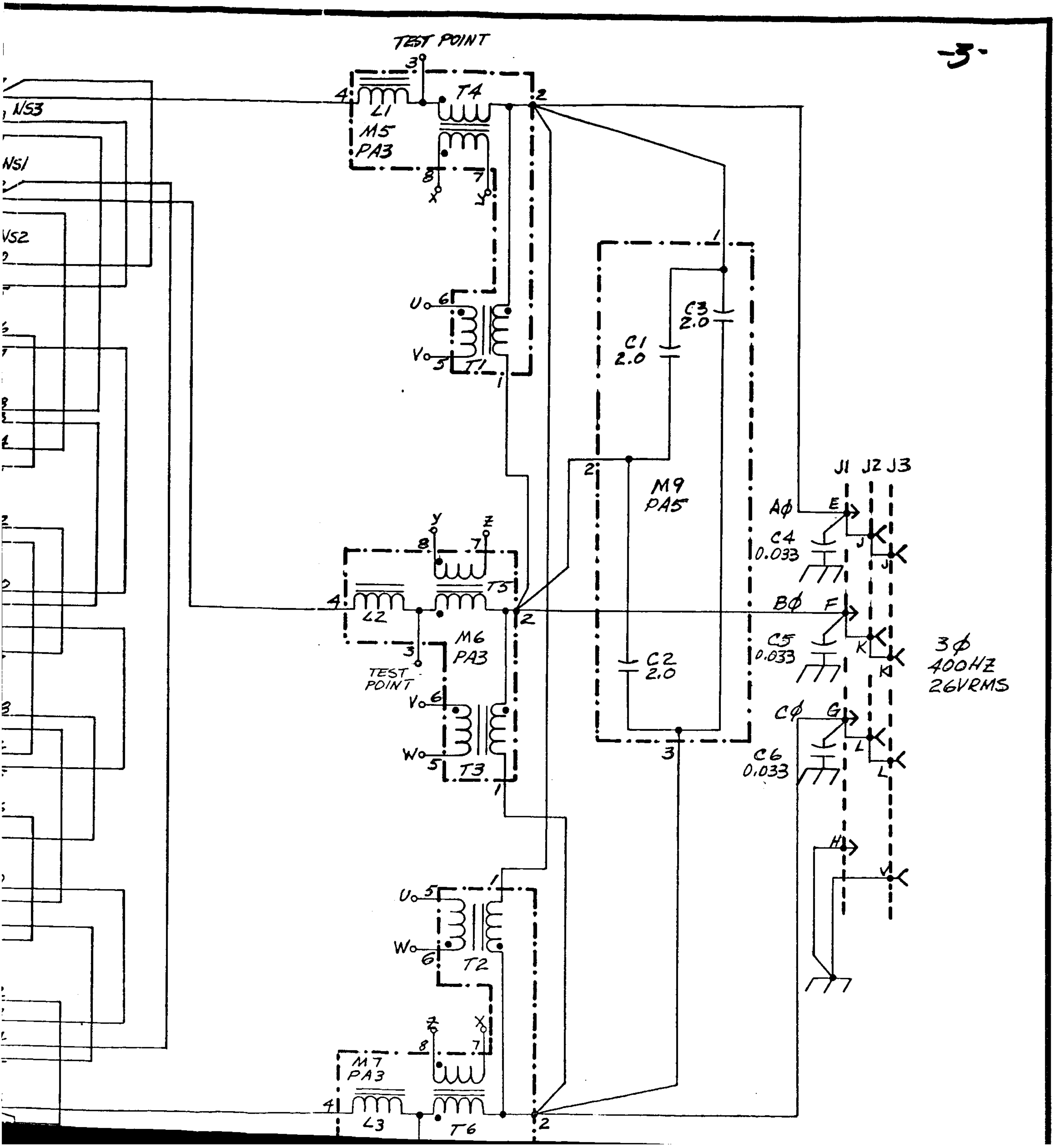
Electrical Specifications for L-169

NOTES:

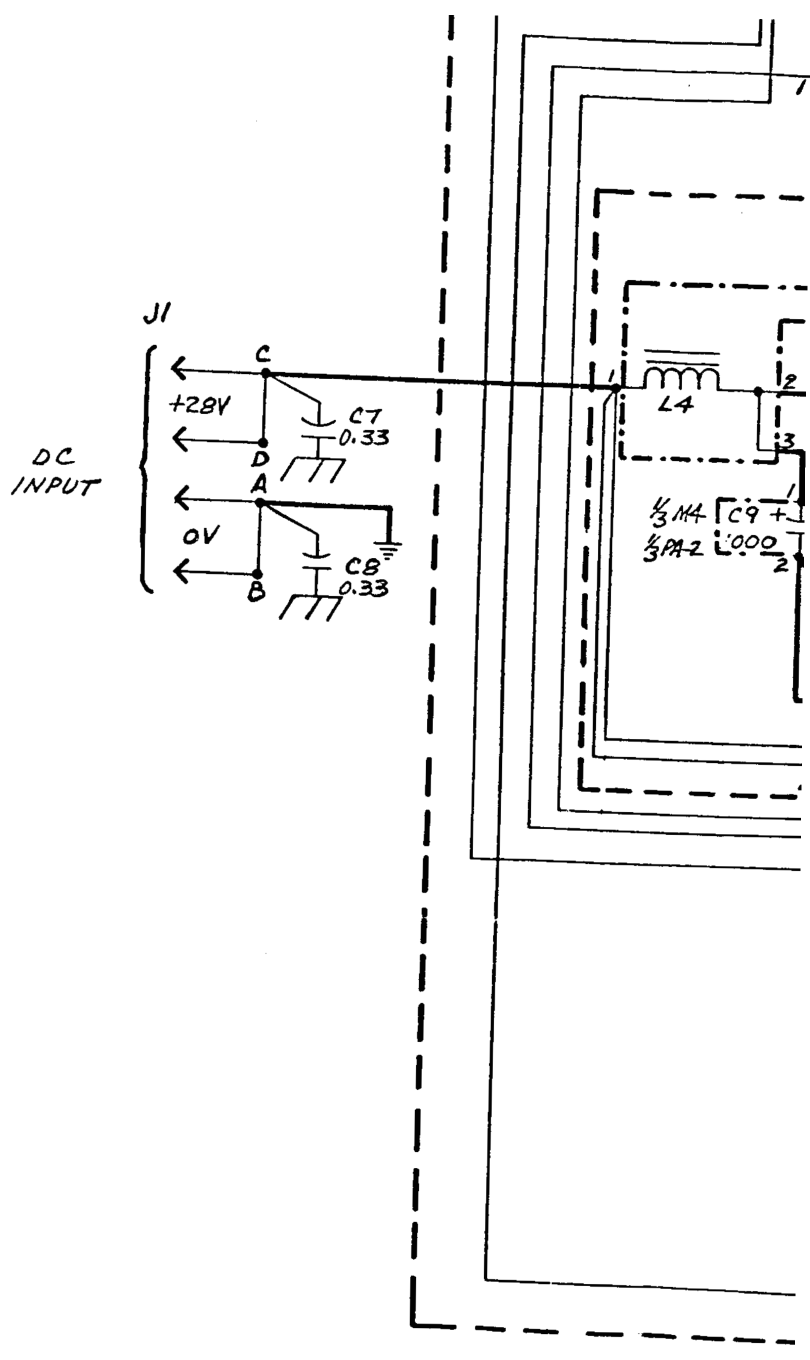
1. ALL RESISTORS ARE 1/8W AND EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE NOTED.
3. ALL HOOKUP WIRE INDICATED BY HEAVY LINES IS 18 AWG TEFLON COATED WIRE; ALL OTHER HOOK UP WIRE IS 22 AWG TEFLON COATED WIRE UNLESS NOTED OTHERWISE.
4. CIRCUITRY ENCLOSED BY HEAVY DASHED LINES INDICATES CIRCUITRY MOUNTED ON PRINTED CIRCUIT BOARDS. — — — —
5. POTTED ASSEMBLIES HAVE THEIR CIRCUITRY ENCLOSED BY —·—·—·—
6. CIRCUITRY ENCLOSED BY —··—··—··— REPRESENTS "SINGLE PACKAGE" CIRCUITRY.



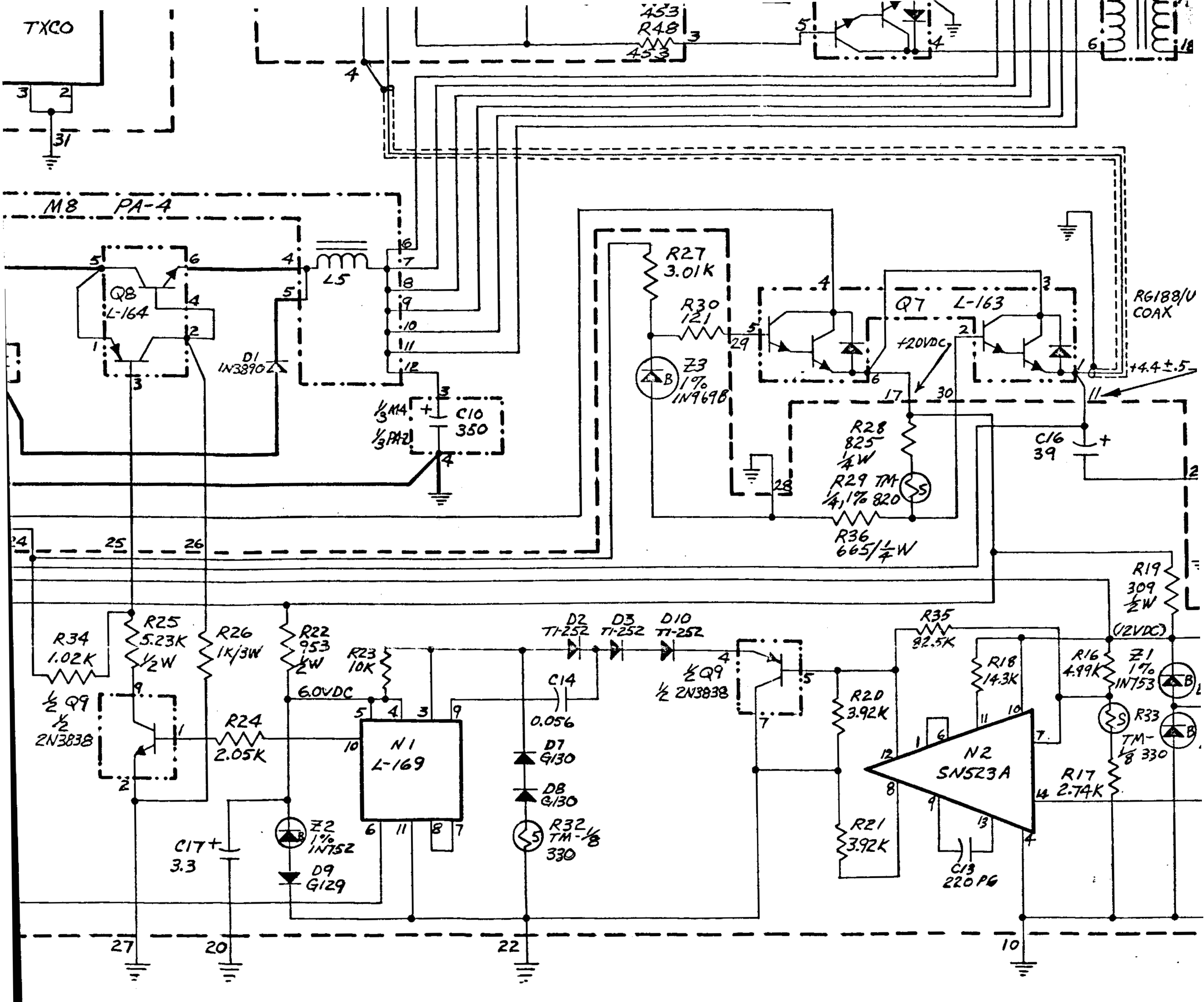

W LEVEL CIRCUITRY
C. BOARD
JOHNSON COUNTER P.C. BOARD
C12
39
N4
SN5300
N3
SN5311
N5
SN5302
N6
SN5302
N7
SN5302
NA3
L-168
NA4
L-167
NA1
L-166
RG188/U
9.6KHZ
R37
453
R38
453
R39
453
R40
453
R41
453
R42
453
R43
453
R44
453
R45
453
R46
453
R47
Q1
L-163
Q2
L-163
Q3
L-163
Q4
L-163
Q5
L-163
Q6
L-163
T7
M1
PA1
T8
T9
M2
PA1
T10
T11
M3
PA1
T12



TEST POINT
L1
T4
M5
PA3
NS3
NS1
NS2
T1
M9
PA5
C1
2.0
C2
2.0
C3
2.0
J1 J2 J3
Aφ
Bφ
Cφ
C4
0.033
C5
0.033
C6
0.033
3φ
400HZ
26VRMS
L2
T5
M6
PA3
TEST POINT
T3
T2
M7
PA3
L3
T6


J1
C
+28V
C7
0.33
D
DC
INPUT
A
0V
C8
0.33
B
L4
1
2
3
1/3 M4
1/3 PA-2
C9
+
1000
1
2

SC06031


TXCO
R48
453
M8 PA-4
Q8
L-164
D1
1N3890
L5
C10
350
1/3 M14
1/3 PA2
R27
3.01K
R30
121
Z3
1%
1N969B
Q7 L-163
+20VDC
R28
825
1/4W
R29 TM-
1/4, 1% 820
R36
665/1/4W
RG188/U
COAX
+4.4±.5
C16
39
R19
309
1/2W
R34
1.02K
R25
5.23K
1/2W
R26
1K/3W
R22
953
1/2W
R23
10K
6.0VDC
1/2 Q9
1/2 2N3838
R24
2.05K
N1
L-169
D2
T1-252
D3
T1-252
D10
T1-252
C14
0.056
D7
G130
D8
G130
R32 TM-1/8
330
Z2
1%
1N752
D9
G129
C17
3.3
R35
82.5K
(12VDC)
R18
14.3K
R16
4.99K
Z1
1%
1N753
R33
TM-1/8 330
R20
3.92K
R21
3.92K
N2
SN523A
C13
220 PF
R17
2.74K

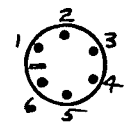
TEST POINT

ALL	U	POINTS	ARE	COMMON
"	V	"	"	"
"	W	"	"	"
"	X	"	"	"
"	Y	"	"	"
"	Z	"	"	"

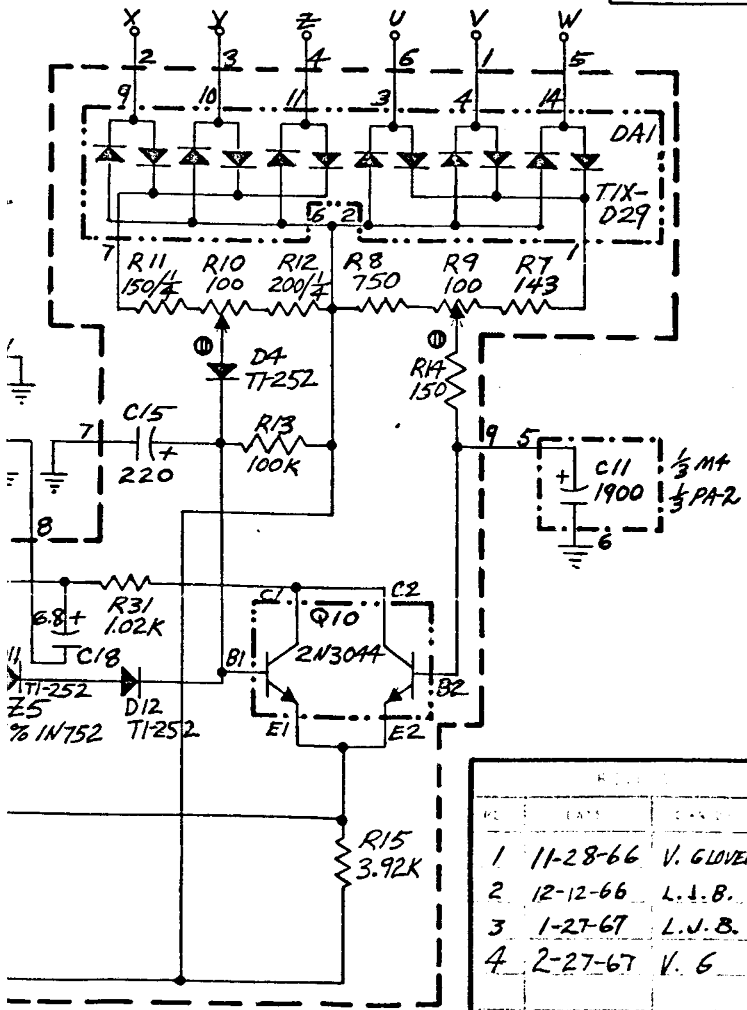
CHASSIS GROUND

-28V TERMINAL

L-163, L-164 PIN NUMBERING SYSTEM:



TOP VIEW



1	11-28-66	V. GLOVER	V.G.
2	12-12-66	L.J.B.	V.G.
3	1-27-67	L.J.B.	V.G.
4	2-27-67	V. G	V.G.

TEXAS INSTRUMENTS INCORPORATED

75 VA STATIC INVERTER MODEL A SCHEMATIC AND WIRING DIAGRAM

V.G.
V.G. 11-2-66